Cell Broadband Engine Architecture

Patrick White
Aun Kei Hong
Overview

• Background
• Goals
• Components
  – PPE
  – SPE
  – EIB
  – Memory I/O
  – PMU, TMU

• Overall Chip Specifications
• Commercialization
• Conclusion
Background

- Ken Kutaragi
- Sony, IBM, and Toshiba Partnership
- 400+ people and $400M
- 10 centers globally
Goals

• Parallelism
  – Thread Level
  – Instruction Level
  – Data Level

• Create a computer that acts like cells in a biological system
POWER Processing Element (PPE)

- Power Processing Unit (PPU)
- Cache
  - 32 kB L1 Cache
  - 512 kB L2 Cache
- SIMD (Single Issue Multiple Data)
  - Vector multimedia extension
- Controls SPEs
POWER Processing Unit (PPU)

• Main processor
• Dual issue, In order, Dual thread
SPE: Synergistic Processing Element
SPU: Synergistic Processing Unit
MFC: Memory flow controller
LS: Local store
Synergistic Processing Element (SPE)

- Synergistic Processing Unit
- Memory Flow Controller
- Direct Memory Access
Synergistic Processing Unit (SPU)

- Dual issue, in order
- 256 kB embedded SRAM
- 128 entry operations per cycle
Memory Flow Controller (MFC)

- Connects SPE to EIB
- Communicates through SPU channel interface
- Process commands by depending on the type of commands
- Process DMA Commands
SPE: Synergistic Processing Element
SPU: Synergistic Processing Unit
MFC: Memory flow controller
LS: Local store
Element Interconnect Bus (EIB)

- Facilitates commutation between the PPE, SPE, Main Memory, and I/O
- 4 16-bit wide data rings
- Allows up to 3 concurrent transfers
- Contains a data bus arbiter that decides which ring handles each request
- Runs on half the processor speed
Memory Interface Controller (MIC)

• Interface between main memory and the Cell
• Two Rambus XRD memory banks
  – 36 bits wide
  – Independent control bus
• Banks are interleaved in address space
• Configurable to run just one bank
Bus Interface Controller (BIC)

- Two Flexible interfaces
  - Varying Protocols
  - Varying Bandwidth

- Configurable
  - Two IO interfaces (OIIF 0/1)
  - IOIF and Broadband Interface (BIF)
Broadband Interface (BIF)

- Permits two Cells to be connected both PPE and all SPE’s
- Will use the IOIF0 of both chips
Power Management Unit
- Allows software control of chip power
- By Throttling, pausing, or Stopping
  - Single element
  - Multiple elements
  - Entire Chip

Thermal Management Unit
- Contains
  - Linear Sensor placed at a location to get the global temperature
  - Digital Thermal Sensors (DTS)
    - One at the PPU
    - One at each element
    - One at the Linear Sensor
Chip Specifications

- Greater than 4 GHz clock speed
- Greater than 256 GFLOPS single precision
- Greater than 26 GFLOPS double precision
- Area 221 mm$^2$
- 90 nm technology
- I/O bandwidth of 76.8 Gbytes/sec
- Power 60-80 Watts
Commercialization

- Sony PS3
- IBM servers
- Toshiba Blue-ray, HDTV, DVD player, etc
Roadrunner

• As of June 2010 it is the 3rd best supercomputer in the world, was the best when it was made in 2008

• 12,960 Cell processors on IBM QS22 blades

• Was the first to Brake the petaflop barrier on May 25, 2008 (on its 3rd try)

• Is used for
  • national security problems
  • test nuclear stockpiles
  • run annual testing of various nuclear weapon systems
  • predict long-term climate change
  • studying the universe
  • trying to find an HIV vaccine
Thanks for Not Sleeping

Questions?