AMD APU series

Connor Goss, Jefferson Medel
Agenda

➢ Overview
➢ APU vs. CPU+GPU
➢ Graphics Engines
➢ CPU Architecture
➢ Future
Overview

- What is an APU?
  - Accelerated Processing Unit
  - A processor that combines CPU and GPU elements into a single architecture
- APU brand of AMD, Intel uses different name
- Why APU?
  - Able to perform tasks of both a CPU and GPU with less space and power.
  - At cost of performance compared to high end individual units
  - Sufficient for majority of computers
Essentially...

- CPUs use serial data processing
- GPUs use parallel data processing

[Image: THE AMD FUSION FAMILY OF ACCELERATED PROCESSING UNITS]

History

- Single Core
  - Limitations
    - Speed
    - Power
    - Complexity

- Multi Core
  - Limitations
    - Power
    - Scalability

- Heterogeneous
  - CPU and GPUs designed separately do not work optimally together
  - Graphics Capability included in chip rather than in chipset
Bandwidth

BANDWIDTH CONSTRAINTS IN IGP CHIPSETS

Heterogeneous System Architecture

http://developer.amd.com/resources/heterogeneous-computing/what-is-heterogeneous-system-architecture-hsa/
Iterations

➢ Desktop Processors
  ○ Llano - Trinity - Richland - Kaveri

➢ Server Processors
  ○ Kyoto

➢ Mobile
CPUs and GPUs

- Different Design Goals
  - CPUs are based on maximizing performance of a single thread
  - GPUs maximize throughput at cost of individual thread performance
- CPU
  - Dedicated to reduce latency to memory
- GPU
  - Focus on ALU and registers
  - Focus on covering latency
Graphics Engine

➢ Based on AMD/ATI Radeon HD series
➢ TeraScale architecture
  ○ Early APUs
➢ Graphics Core Next
  ○ Current architecture
TeraScale Architecture

- Developed by AMD implementing the unified shader model following Xenos to compete with Nvidia’s unified shader microarchitecture Tesla
- Replaced old fixed-pipeline microarchitectures
- Eventually also used by Intel in the HD 2000+ series
- Succeeded by Graphics Core Next in 2011
Graphics C

http://www.neoseeker.com/Articles/Hardware/Reviews/AMD_HD_7950/2.html
Compute Unit

- Branch & Message Unit
- Scheduler
- Vector Units (4x SIMD-16)
- Vector Registers (4x 64KB)
- Local Data Share (64KB)
- Scalar Unit
- Scalar Registers (4KB)
- Texture Fetch
- Texture Filter Load / Store Units (4)
- Texture Fetch Load / Store Units (16)
- L1 Cache (16KB)
Graphics Core Next

- System memory bus
  - Copy entire data
  - 128-bit DDR3-2133 = 34.13 GB/s
  - Latency: unknown

- System memory

Memory controller
MMU
cache hierarchy

CPU
GPU

Memory controller
MMU
cache hierarchy

CPU
GPU
CPU Architecture (Llano)

➢ Bulldozer architecture
➢ 32nm technology
➢ 2-4 Modules (4-8 Cores)
➢ Module rather than Core
  ○ 2 integer ALU per module
  ○ 1 FP per module
➢ Poor single-threaded performance
CPU Architecture (Trinity)

- Piledriver architecture
- Incremental changes
- 1-2 Modules (2-4 Cores) on APU
- 2-4 Modules (4-8 Cores) on non-APU
- Better single-threaded performance, still behind Intel
CPU Architecture (Kaveri)

➢ Steamroller architecture
➢ Unified Video Decoder, Video Codec Engine
➢ Support hybrid model, discrete+integrated
➢ Graphics Core Next
  ○ 3-8 Compute Units
Heterogeneous Evolution

Comparison to Intel

AND NOW THE APU IS EVERYWHERE

“SANDY BRIDGE”  “IVY BRIDGE”  “HASWELL”  ELITE AMD A-SERIES / CODENAMED “RICHLAND”

Balanced architectures are the future of parallel computing
Open CL™ is the future of parallel computing
A strong GPU is about:
- Gaming
- Compute
- Imaging
- Video

(DirectX®, OpenGL)
(Open CL™)
(Adobe)
(.mkv, Transcode)

Future Roadmap

➢ Excavator architecture
  ○ 2015 release
  ○ Final architecture based on Bulldozer
  ○ 30% more efficient

➢ AMD K12 architecture
  ○ 2016 release
Future Roadmap

- HSA Foundation

HSA Solution Stack

HSA Platform

CPU

GPU

ACC

OS

HSA Runtime Infrastructure

LLVM Compiler
HSAIL Finalizer
AQL – Architected Queuing Language

HSA Accelerated Applications
Access to Broad Set of Programming Languages

Legacy Applications

Software Innovation

Hardware Innovation

http://developer.amd.com/resources/heterogeneous-computing/what-is-heterogeneous-system-architecture-hsa/
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