ALTERNATIVE RAM DESIGNS

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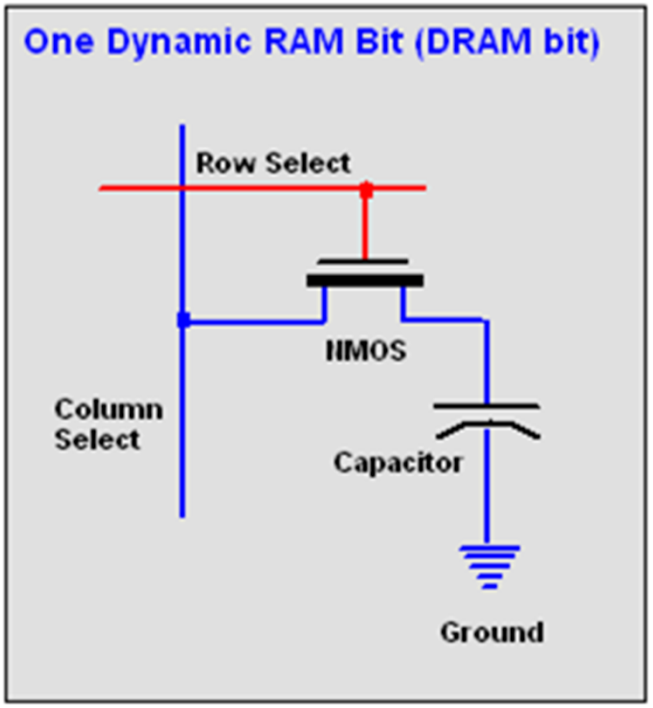
AGENDA

1. Review of SRAM & DRAM as benchmarks
2. MRAM (Magnetoresistive)
3. TRAM (Thyristor)
4. ZRAM (Zero-capacitor)
5. Summary
6. Questions

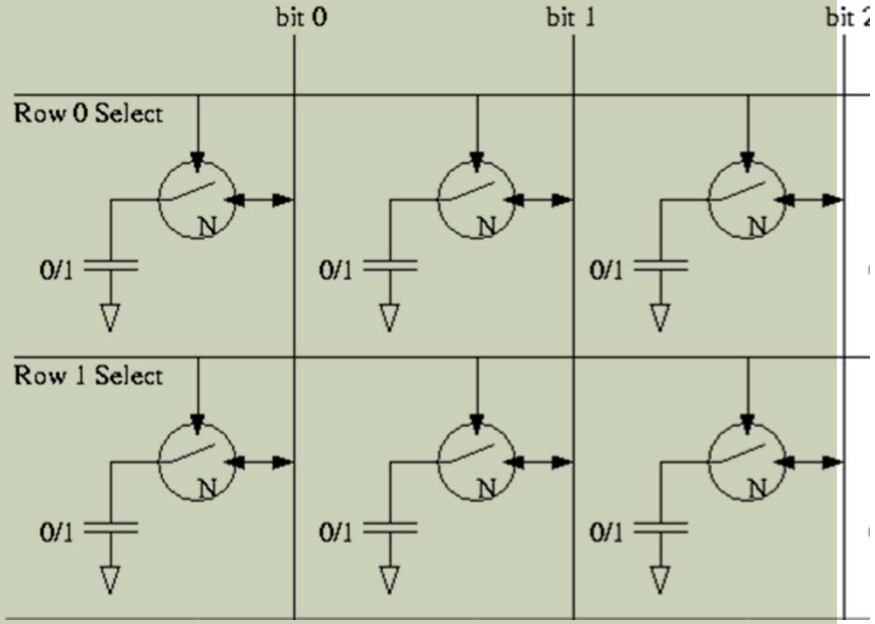
DYNAMIC RAM (DRAM)

- Simple, low-cost, high-density, and Volatile
- Consists of 1 transistor & 1 capacitor per memory cell
- Digital value of cell is stored on the capacitor
- As time passes, the capacitors are discharged, requiring constant refreshing (usually every <64ms) making this type of memory Dynamic.



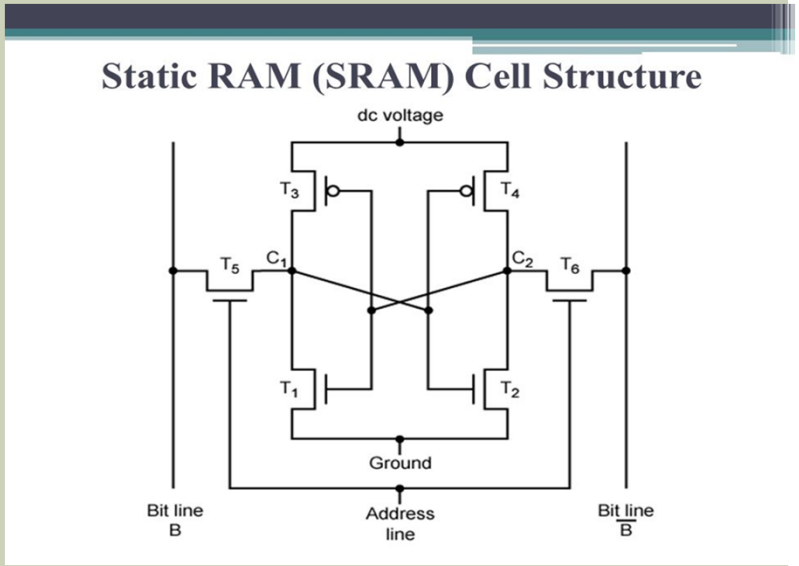
DYNAMIC RAM (DRAM)

- Due to the need to refresh each cell regularly, power consumption is fairly high
- Due to the small cell size, scaling blocks to large capacity keeps speed high as shorter trace lengths keep latency down



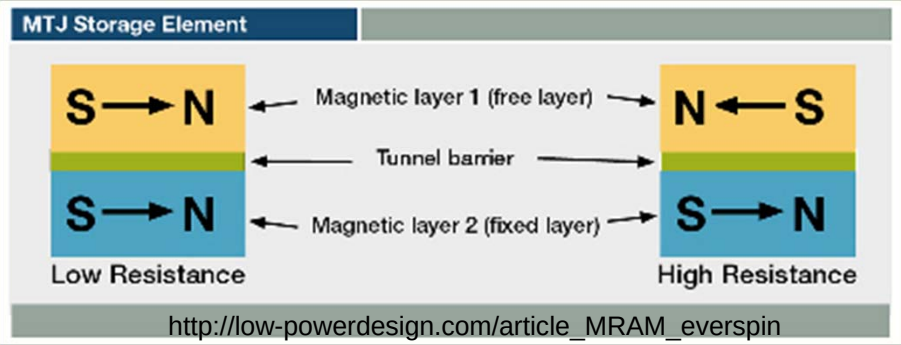
STATIC RAM (SRAM)

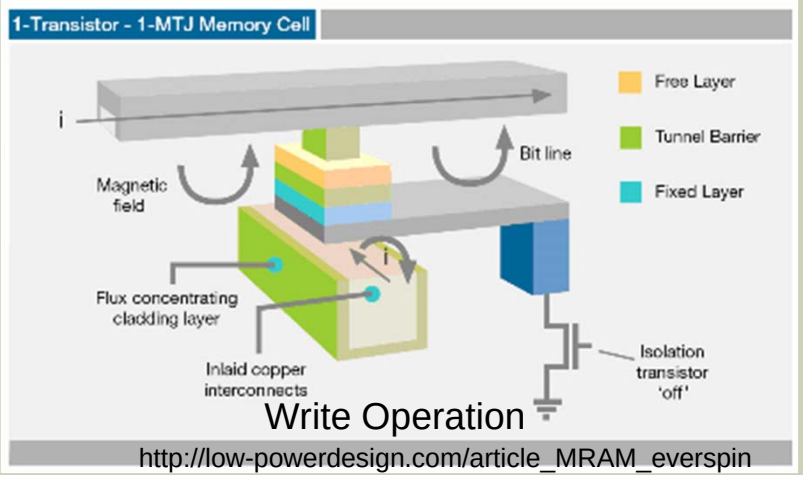
- Volatile
- Typically uses 6-8 transistors
- Faster than DRAM
- Larger than DRAM
- Cache closer to CPU (L2/L3) than DRAM
- No refresh required (less power!)
- Power can be less than DRAM depending on frequency



MAGNETORESISTIVE RAM (MRAM)

- Non-volatile, solid state - magnetic storage
- Built from two ferrous plates with an insulating layer
  - One plate is kept charged at a constant level, the other is varied
  - Reading occurs by sending a (small) test current through the cell (tunnel magnetoresistance)
  - Variety of write methods include a system similar to Core Memory (1960s)
- Writes can be **costly**
- Density adds complexity & concerns



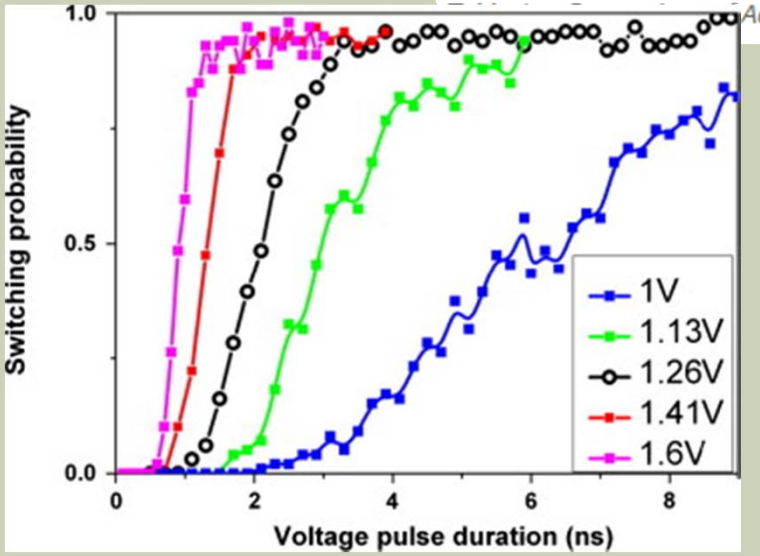


MRAM

	MRAM (180 nm)	MRAM (65nm)	Spin-Torque MRAM (65 nm)	Flash (65 nm)	DRAM (65 nm)	SRAM (65 nm)
Cell Size (um2)	1.25	0.16	0.04	0.04	0.03	0.3
Read Time	35 ns	10 ns	10 ns	10 - 50 ns	10 ns	1 ns
Program Time	5 ns	5 ns	10 ns	0.1-100 ms	10 ns	1 ns
Program Energy/bit	150 pJ	100 pJ	1 pJ	10,000 pJ	5 pJ	5 pJ
Endurance	> 1015	> 1015	>1015	105 write	>1015	>1015
Non-volatility	YES	YES	YES	YES	NO	NO

Advanced Memories

http://low-powerdesign.com/article_MRAM_everspin

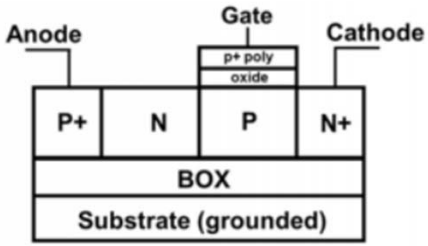


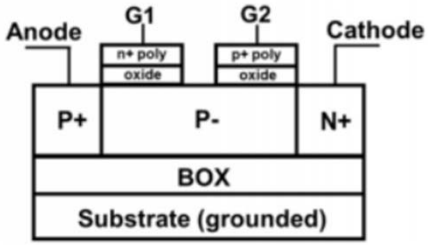
- Advertised size “pros” lead to cons
  - Power & reliability correlate
  - Power & size correlate

http://www.sciencedirect.com/science/article/pii/S0026271412002326

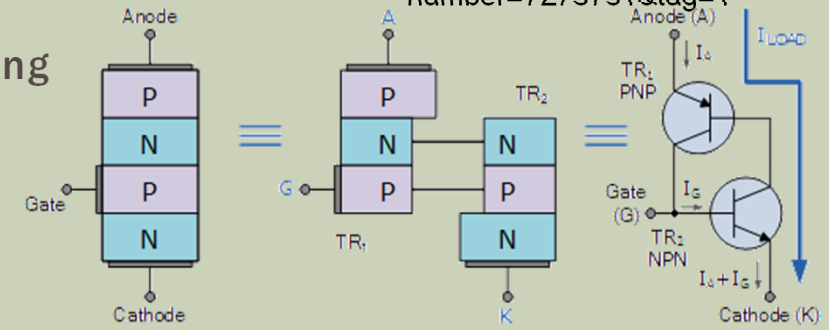
THYRISTOR RAM (TRAM)

- Volatile
- Silicon on Insulator (SOI) pnpn thyristor
- 4x better density than 6T-SRAM
  - Equal speed requires 2.5x higher density
- Better active and standby power than 6T-SRAM
- Fast Write with Thin Capacitively Coupled Thyristor (TCCT-TRAM)
  - Raises scalability concerns (high doping precision)
- S and D T-RAM variants exist
  - Compatible with FinFET and other technologies





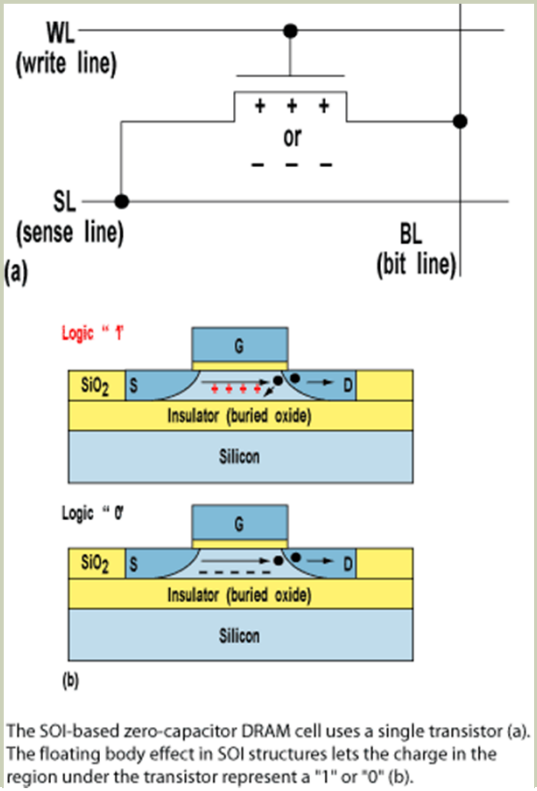
http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7273751&tag=1



http://www.electronics-tutorials.ws/power/thyristor.html

ZERO-CAPACITOR RAM (ZRAM)

- Silicon on Insulator (SOI) transistor body produces capacitance in the transistor.
  - Exploits “floating body effect” to store information with only one transistor
- Eliminating the capacitor reduces on-chip size, increasing memory density and access speed.
  - Transistor and capacitor are essentially stacked in the Z-plane, increasing density.
  - Shorter trace distance decreases overall latency despite having higher cell access time than SRAM



The SOI-based zero-capacitor DRAM cell uses a single transistor (a). The floating body effect in SOI structures lets the charge in the region under the transistor represent a "1" or "0" (b).

ZERO-CAPACITANCE RAM (Z-RAM)

- Speed increases over SRAM occur at larger memory block sizes
- Writes occur using only gate and drain
- Writes occur during ON state (consumes power!)
- Licensed by AMD, though has not been brought into production

COMPARISON SUMMARY

	DRAM	SRAM	MRAM	TRAM	ZRAM	Flash
Refresh Required	Yes	**No**	**No**	Varies	Yes	No
Density	High 1T + 1C	Low 6T	High ~2T	High ~3T	**Very High** **1T**	High 1T
Volatile	Yes	Yes	**No**	Yes	Yes	No
Speed	High	Very High	High	**High / Very High**	**High / Very High**	Very Low
Scalability	**High**	Low	Varies	Varies / High	**High**	High
Power	Less	More	**Much Less**	Varies / Less	More	Much More
Cost	Less	More	More	More	No Production (AMD)	**Much Less**

Slide 11

1 for reference. can use this info, but make full table

Andrew Lints, 12/1/2016

SUMMARY

- Design is the pursuit of the “Holy Grail”
- No one design fits every ideal, so design trade-offs are required
- Key parameters
  - Speed (Read & Write!)
  - Power
  - Reliability (Accurate read, write & maintenance of value)
  - Volatility
  - Die Size & Density
  - Scalability
  - Cache Level (on, off chip?)
- Watch for the 3D stacked RAM project group!

QUESTIONS?

WORKS CITED

- http://ieeexplore.ieee.org/document/4655409/?arnumber=4655409 (ZRAM)
- http://www.hotchips.org/wp-content/uploads/hc_archives/hc19/3_Tues/HC19.05/HC19.05.02.pdf (TRAM)
- http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7273751 (TRAM)
- http://nve.com/Downloads/mram.pdf (MRAM)
- http://low-powerdesign.com/article_MRAM_everspin (MRAM)
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- http://www.embedded.com/design/real-time-and-performance/4026000/The-future-of-scalable-STT-RAM-as-a-universal-embedded-memory (MRAM focus, others mentioned/benchmarked)
- http://www.digitimes.com/bits_chips/a20060328PR202.html (ZRAM)
- http://searchsolidstatestorage.techtarget.com/answer/Comparing-performance-and-cost-of-DRAM-vs-NAND (Flash/DRAM)
- http://hexus.net/tech/news/ram/98035-kilopass-dram-uses-vlt-tech-eliminate-refresh-requirement/ (DRAM)
- http://www.digitimes.com/bits_chips/a20060328PR202.html (ZRAM)
- Lecture by Dr. Shaaban (http://meseec.ce.rit.edu/cmpe550-fall2016/550-11-14-2016.pdf) (SRAM & DRAM)
- http://www.diffen.com/difference/Dynamic_random-access_memory_vs_Static_random-access_memory#Power_Consumption (D & SRAM)
- https://pdfs.semanticscholar.org/7e41/2ed88bb7855600a63fe7c5b91af7b1610726.pdf (SRAM)