ALTERNATIVE RAM DESIGNS

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AGENDA

1. Review of SRAM & DRAM as benchmarks
2. MRAM (Magnetoresistive)
3. TRAM (Thyristor)
4. ZRAM (Zero-capacitor)
5. Summary
6. Questions
DYNAMIC RAM (DRAM)

- Simple, low-cost, high-density, and Volatile
- Consists of 1 transistor & 1 capacitor per memory cell
- Digital value of cell is stored on the capacitor
- As time passes, the capacitors are discharged, requiring constant refreshing (usually every <64ms) making this type of memory Dynamic.
- Due to the need to refresh each cell regularly, power consumption is fairly high.
- Due to the small cell size, scaling blocks to large capacity keeps speed high as shorter trace lengths keep latency down.
STATIC RAM (SRAM)

- Volatile
- Typically uses 6-8 transistors
- Faster than DRAM
- Larger than DRAM
- Cache closer to CPU (L2/L3) than DRAM
- No refresh required (less power!)
- Power can be less than DRAM depending on frequency
MAGNETORESISTIVE RAM (MRAM)

- Non-volatile, solid state - magnetic storage
- Built from two ferrous plates with an insulating layer
  - One plate is kept charged at a constant level, the other is varied
  - Reading occurs by sending a (small) test current through the cell (tunnel magnetoresistance)
  - Variety of write methods include a system similar to Core Memory (1960s)
- Writes can be costly
- Density adds complexity & concerns
MRAM

- Advertised size “pros” lead to cons
  - Power & reliability correlate
  - Power & size correlate


http://low-powerdesign.com/article_MRAM_everspin
THYRISTOR RAM (TRAM)

- Volatile
- Silicon on Insulator (SOI) pn-pn thyristor
- 4x better density than 6T-SRAM
  - Equal speed requires 2.5x higher density
- Better active and standby power than 6T-SRAM
- Fast Write with Thin Capacitively Coupled Thyristor (TCCT-TRAM)
  - Raises scalability concerns (high doping precision)
- S and D T-RAM variants exist
  - Compatible with FinFET and other technologies

[Diagram: Thyristor RAM (TRAM) and Willard-Norton Thyristor]

http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7273751&tag=1
http://www.electronics-tutorials.ws/power/thyristor.html
ZERO-CAPACITOR RAM (ZRAM)

- Silicon on Insulator (SOI) transistor body produces capacitance in the transistor.
  - Exploits “floating body effect” to store information with only one transistor
- Eliminating the capacitor reduces on-chip size, increasing memory density and access speed.
  - Transistor and capacitor are essentially stacked in the Z-plane, increasing density.
  - Shorter trace distance decreases overall latency despite having higher cell access time than SRAM

The diagram shows the SOI-based zero-capacitor DRAM cell uses a single transistor (a). The floating body effect in SOI structures lets the charge in the region under the transistor represent a "1" or "0" (b).
ZERO-CAPACITANCE RAM (Z-RAM)

- Speed increases over SRAM occur at larger memory block sizes.
- Writes occur using only gate and drain.
- Writes occur during ON state (consumes power!)
- Licensed by AMD, though has not been brought into production.
## COMPARISON SUMMARY

<table>
<thead>
<tr>
<th></th>
<th>DRAM</th>
<th>SRAM</th>
<th>MRAM</th>
<th>TRAM</th>
<th>ZRAM</th>
<th>Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Refresh Required</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Varies</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td>Density</td>
<td>High 1T + 1C</td>
<td>Low 6T</td>
<td>High ~2T</td>
<td>High ~3T</td>
<td>Very High 1T</td>
<td>High 1T</td>
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<tr>
<td>Volatile</td>
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<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td>Speed</td>
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<td>Very High</td>
<td>High</td>
<td>High / Very High</td>
<td>High / Very High</td>
<td>Very Low</td>
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<tr>
<td>Scalability</td>
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<td>Low</td>
<td>Varies</td>
<td>Varies / High</td>
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<td>High</td>
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<tr>
<td>Power</td>
<td>Less</td>
<td>More</td>
<td>Much Less</td>
<td>Varies / Less</td>
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<td>Much More</td>
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<tr>
<td>Cost</td>
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<td>More</td>
<td>More</td>
<td>More</td>
<td>No Production (AMD)</td>
<td>Much Less</td>
</tr>
</tbody>
</table>
for reference. can use this info, but make full table
Andrew Lints, 12/1/2016
Design is the pursuit of the “Holy Grail”
No one design fits every ideal, so design trade-offs are required
Key parameters
- Speed (Read & Write!)
- Power
- Reliability (Accurate read, write & maintenance of value)
- Volatility
- Die Size & Density
- Scalability
- Cache Level (on, off chip?)
Watch for the 3D stacked RAM project group!
Works Cited

- [http://www.difffen.com/difference/Dynamic_random-access_memory_vs_Static_random-access_memory#Power_Consumption](http://www.difffen.com/difference/Dynamic_random-access_memory_vs_Static_random-access_memory#Power_Consumption) (D & SRAM)
- [https://pdfs.semanticscholar.org/7e41/2ed88bb7855600a63fe7c5b91af7b1610726.pdf](https://pdfs.semanticscholar.org/7e41/2ed88bb7855600a63fe7c5b91af7b1610726.pdf) (SRAM)