Architecture of the Super NES

Jacob Klassen & Thomas Papish
Overview - Super Nintendo Entertainment System

- **SNES: 16-bit Gaming Console**
  - Computer with interchangeable ROM for game data
  - Processes read-in game data alongside controller inputs to output video and audio
- **Lifespan:** 1991-1999
- Proceeded the 8-bit NES (1980’s)
- Competed against the 32-bit Sega Genesis
Three Main Processing Units:

- Central Processing Unit (CPU)
- Picture Processing Unit (PPU)
  - Split into PPU1 & PPU2
- Audio Processing Unit (APU)
Central Processing Unit: Ricoh 5A22

- Based on a 16-bit 65c816 core
- Input Clock Rate: 21.47727MHz
- Clock divider of 6, 8, or 12 for the bus clock rate
- 24-bit and 8-bit address buses
- 8-bit data bus
- Peaks at 1.79 MIPS; averages 1.5 MIPS
- Direct Memory Access: 2.68MB/s
- 16-bit multiplication & division unit
- 128kB of RAM for register addressing
- Used 65816 ISA (similar to Assembly)
  - 1 word per instruction: 1-byte opcode, 0-3 byte operand
Central Processing Unit: Bus Connections

Blue: 24-bit CPU Address “A” Bus
Pink: 8-bit CPU Address “B” Bus
Yellow: 8-bit CPU Data Bus
Picture Processing Unit

- Two closely tied IC blocks: PPU1 and PPU2
- Resolutions: 256x224, 256x239, 512x224, 512x239
  - 512 x 224 and 521 x 476 also possible through interlaced graphics
- 15-bit color space = 32,768 possible colors
- Upto 4 background layers and 128 sprites on screen
- VRAM of 64 kB
- 8 modes of display
  - Modes use different combinations of backgrounds and palettes
  - Certain modes are dedicated to scrolling, scaling, and rotation

<table>
<thead>
<tr>
<th>Mode</th>
<th># Colors for BG</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>4 4 4 4</td>
</tr>
<tr>
<td>1</td>
<td>16 16 4 -</td>
</tr>
<tr>
<td>2</td>
<td>16 16 - -</td>
</tr>
<tr>
<td>3</td>
<td>256 16 - -</td>
</tr>
<tr>
<td>4</td>
<td>256 4 - -</td>
</tr>
<tr>
<td>5</td>
<td>16 4 - -</td>
</tr>
<tr>
<td>6</td>
<td>16 - - -</td>
</tr>
<tr>
<td>7</td>
<td>256 - - -</td>
</tr>
<tr>
<td>7EXTBG</td>
<td>256 128 - -</td>
</tr>
</tbody>
</table>


Picture Processing Unit - Example of Mode 1

Mode 1 uses:

- 3 background layers
- 1 Sprites layer

General Priority:

- BG3
- Sprites
- BG1
- BG2

Normal View
Picture Processing Unit - Example of Mode 1

BG1

BG2

BG3

Sprites
Audio Processing Unit

- Controller
- Joy Stick
- Game Cassette
- TV
- Stereo, etc.
- Main-CPU Side
- SNES CPU
- SNES PPU
- SNES Bus
- SNES Sound Side
- Sound CPU
- DSP
- DAC Converter
- 512K RAM
Audio Processing Unit

- Consists of a 8-bit Sony SPC700 Processor and a 16-bit Digital Signal Processor
- Audio RAM of 64 kB
- Clock Rate: 24.576 MHz
- DSP uses 8 independent voices and an FIR filter to generate needed sounds
- Very independent - only communicates with CPU via 4 registers and sometimes with the game cartridge
Game Pak

- Served as the ROM of the console
- Capacity of 117.75MBits
- CPU, PPU, and APU interact with the cartridge
- Can include additional hardware to support the game:
  - Battery-backed SRAM for saving the game’s state
  - Additional RAM to supplement the console’s native RAM
  - Enhancement chips to operate in-parallel with the native processors
- Design Limitations:
  - Data transfer speed between the console and the cartridge
  - Current limit of the console to supply power to the cartridge
Game Pak - Enhancement Chips

Design Philosophy: Allow cartridges to interface supporting hardware rather relying solely on an expensive CPU that would become obsolete in a few years.
Enhancement Chips: Super FX

- 16-bit supplemental RISC CPU acting as a graphics accelerator chip
- Main Draw: Rendering 3D polygon graphics
- Assisted the console’s processors in rendering advanced 2D effects
- Allowed additional foreground and background layers
- Able to render larger sprites and objects on screen
Enhancement Chips: DSP-1

- Fixed-point Digital Signal Processor unit to supplement graphical calculations
- Fast vector-based calculations, bitmap conversions, 2D-3D coordinate transformations
- Used as math coprocessor for games needing advanced screen scrolling, scaling, and rotation
Enhancement Chips: Super Accelerator 1 (SA1)

- CPU also based on the 65c186 core
- Operates alongside, rather than under, the console’s CPU
- Several improvements over 65c186 core:
  - 10.74 MHz clock speed
  - Faster RAM and 2kB of internal RAM
  - Memory-mapping capabilities
  - Bitmap to bitplane transfer
  - PPU-synched hardware timers
Controllers

- Standard Controller data is fed directly to the CPU with 1 bit for each switch on the controller
- Super NES Mouse - substituted for standard controller
  - Three tracking speeds
- Super NES Super Scope - used infrared beams to detect colors on the screen
Use of SNES Architecture (2000’s and beyond)

- Emulation: ROM data can be loaded on computer programs designed to simulate the behavior of the console
  - Some designed for accuracy, while others designed for modern performance
- SNES Classic: Nintendo released a miniature “plug-and-play” computer with a built-in set of SNES games
  - Used modern hardware to mimic the behavior of the SNES
  - No cartridges; stored game data on internal memory
  - Came with additional features such as save-states on-command
- SNES Modding Communities:
  - Several online documents preserved 15+ years after its lifespan for hardware modifications, software development using the 65c186 ISA, or simulated recreations of the architecture (Arduino & other microprocessors, FPGAs, etc.)
References

- https://i.ytimg.com/vi/VFNjUx50wME/hqdefault.jpg
- https://images.lukiegames.com/t_300e2/assets/images/snes/snes_orig_ctl_p_yvn1uo.jpg
- http://www.8-bitcentral.com/nintendo/snes.html#specs
- https://wiki.superfamicom.org/65816-reference