HyperTransport

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What is HyperTransport (HT)?

- A point-to-point interconnect technology that links processors to other processors, coprocessors, I/O controllers, and peripheral controllers.
How Does HyperTransport Work?

- **Point-to-Point Link Topology**
  - Structure of the link
- **Electrical/Signal Characteristics**
  - Physical Characteristics of the signal interface
- **Packet Protocols**
  - How data is organized and transferred across the link
Point-to-Point Link Topology

- Employs dual, unidirectional data links with a concise signal set using 1.2V LVDS
- The daisy-chain topology includes a required “host” device and at least one end-point or “cave”.
- Optional:
  - “Tunnel” devices that connect the link to other HT devices
  - “Bridge” devices that interface with non-HT interconnect technologies.
Point-to-Point Link Topology

HyperTransport I/O Device Configurations

- **"Cave" Single-Link**
  - Host
  - Primary
  - Endpoint

- **"Tunnel" Dual-link**
  - Host
  - Primary
  - Secondary
  - Daisy Chain

- **"Bridge" with Tunnel**
  - Host
  - Primary
  - Secondary
  - Multiple Daisy Chains with bridge to other I/O protocols

- **"Bridge" without Tunnel**
  - Host
  - Primary
  - Secondary
  - Daisy Chain

Upstream, Downstream
Electrical/Signal Characteristics

- The unidirectional links include a data path, one or more clock lines, and a single control line.
Electrical/Signal Characteristics

• Each LVDS line is implemented by means of a balanced or differential line
  – Prevents electrical noise from affecting and potentially corrupting the signal detection process

• The HT architectures can be implemented with fewer PCB traces and less signal shielding precautions due to the lower number of signal lines for a given bandwidth.
Electrical/Signal Characteristics

HyperTransport Driver

HyperTransport Receiver

$V_{LDT}$

$R_{ON} \ (DC) \ 50\Omega \pm 10\%$

$R_{LINE} = 60\Omega \pm 10\%$

$R_{TT} \ (DC) \ 100\Omega \pm 10\%$

$V_{LDT}$

$D0$

$D0\#$

$D0$
Packet Protocols

- Command information is transferred as a control packet of 4 or 8 bytes.
- HT data traffic is delivered as a data packet that consists of an 8- or 12-byte header followed by a 4-64 byte data payload.
- For a write request, there is an 8-byte control packet followed by the data packet.
- For a read request, there is an 8-byte control packet, followed by a 4-bytes read response packet, and followed by the data packet.
Packet Protocols

HyperTransport Data Write Sequence

- Write Request Control Packet
  - 8-bytes

- Data Packet
  - 4-64 bytes of data

HyperTransport Data Read Sequence

- Read Request Control Packet
  - 8-bytes

- Read Response Control Packet
  - 4-bytes

- Data Packet
  - 4-64 bytes of data
Packet Protocols

• PRI attaches a high priority request command, consisting of 8-bytes, within a possibly long but lower priority data transfer.
Packet Protocols

• Commands and Data are separated into one of three types of virtual channels:
  – Non-posted requests – require a response from the receiver (all read and some write requests)
  – Posted requests – do not require a response from the receiver (write requests)
  – Responses – replies to non-posted requests (read responses or target done responses to non-posted writes)
History

• Introduced April 2, 2001 by the HyperTransport Consortium
• The Consortium consisted of several initial companies including IBM, Apple and AMD to develop a low latency, royalty free I/O bus design that was high performance and fully scalable
History

• Influential factors: the need for PCI compatibility and a requirement for low cost implementation
  — Conformed to all ordering and enumeration properties of the PCS standard
  — Low cost implementation achieved with the point-to-point link structure and the 1.2V LVDS
Evolution

- Initially started with version 1.0 in 2001 and 1.1 in 2002
  - Max freq. of 800MHz
  - Max bandwidth at 16-bits of 3.2 GB/s
  - Max bandwidth at 32-bits of 6.4 GB/s
  - Max aggregate (bi-directional) bandwidth of 12.8 GB/s
  - DirectPackets Data Streaming (1.1 only)
- Version 2.0 2004
  - Max freq. of 1.4 GHz
  - Max bandwidth at 16-bits of 5.6 GB/s
  - Max bandwidth at 32-bits of 11.2 GB/s
  - Max aggregate (bi-directional) bandwidth of 22.4 GB/s
  - DirectPackets Datastreaming
  - PCI Express Mapping
Evolution

• Version 3.0 in 2006
  – Max freq. of 2.6 GHz
  – Max bandwidth at 16-bits of 10.4 GB/s
  – Max bandwidth at 32-bits of 20.8 GB/s
  – Max aggregate (bi-directional) bandwidth of 41.6 GB/s
  – AC Operation: Capacitive coupling with AC/DC autosensing and autoconfiguration
  – Link splitting
  – Hot-plugging
  – Dynamic link clock/width adjustment
  – DirectPackets Datastreaming
  – PCI Express Mapping
• Version 3.1 2008
  – Max freq. of 3.2 GHz
  – Max bandwidth at 16-bits of 12.8 GB/s
  – Max bandwidth at 32-bits of 25.6 GB/s
  – Max aggregate (bi-directional) bandwidth of 51.2 GB/s
  – Same features as 3.0
Evolution

• Currently at Version 3.1
• Updates approximately every 2 years
• Last revision was 3.10c posted by the Consortium on 5/6/2010
• Small and minor updates in revisions
• The Consortium has stated that its mission is to keep HyperTransport specifications “comfortably” ahead of industry requirements
• HyperShare is also a future concept utilizing the best of interconnect fabric technologies such as HyperTransport, Ethernet and PCI Express
Advantages

- Industry’s lowest latency, highest bandwidth bus for maximum performance
- Processor native (embedded in processor chip) to remove latency from processor to I/O interface control logic found in other standards such as PCI Express
- Native to several companies including AMD, Nvidia and Bay Microsystems
- Low cost
- Royalty free
- Application flexibility (processor to processor, processor to peripheral or I/O and board to board) and excellent scalability
- Low Power consumption
- Backwards compatibility amongst all older versions and transparent extensibility to other standards such as PCI
Disadvantages

• No dedicated I/O address space unlike a PCI bus
• No dedicated configuration address space also unlike a PCI bus
• CPU I/O space is memory-mapped to a high address range
• Addresses must be reserved for I/O and can’t be used for physical storage – may be temporary or permanent
• Two unidirectional LVDS lines are required for every signal line
Applications

• Many companies utilize HyperTransport in their systems including IBM and AMD
• Used in many types of systems including personal computers, super computers and game consoles
• Also used for front-side bus replacement, multiprocessor interconnections, router bus replacement, co-processor interconnections and add-on card connections
Applications

• Two types of HyperTransport cores exist including the standard core and the coherent core

• Coherent core provides similar functionality as the standard core with the ability to connect to coherent devices such as coherent cache (consistent cache blocks in multiprocessing systems)
Conclusion

• Low cost, low latency bus mostly used in front-side bus replacement
• Full backwards compatibility
• Wide array of uses
• Memory-mapped I/O
• Dual unidirectional data links
• Managed by the HyperTransport Consortium
Questions?
References

- General information: [www.hypertransport.org](http://www.hypertransport.org)
- Overview Information: [http://www.hardwaresecrets.com/article/19](http://www.hardwaresecrets.com/article/19)
- HT-Core: [http://ra.ziti.uni-heidelberg.de/coeh/?page=project&id=htcore](http://ra.ziti.uni-heidelberg.de/coeh/?page=project&id=htcore)
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- Connectors: [http://www.hypertransport.org/default.cfm?page=HTConnectorsAndCables](http://www.hypertransport.org/default.cfm?page=HTConnectorsAndCables)