DDR4 SDRAM

Aaron Pulver & Gregg Miller
Overview

- DRAM Basics
- History of DRAM
- DDR4 Improvements
  - Transfer Rates
  - Power Consumption
  - Memory Size
- Future Outlook
DRAM Basics

- Transistor controls trench capacitor
1. The row address must be applied to the address pins. The row must be applied for a certain amount of time before /RAS becomes active.
2. /RAS transitions to low.
3. The column address is applied to the address pins. The column must be applied for a certain amount of time before /CAS becomes active but after /RAS becomes inactive.
4. Write enable must be set low for a certain amount of time (tWP).
5. Data needs to be applied to the data input pins for before /CAS goes low.
6. /CAS must flip from high to low.
7. /CAS and /RAS must return to their inactive states for the cycle to be complete.
DRAM Basic Writing
1. The row address has to be sent to the address pins on the memory controller for the correct amount of time before /RAS goes low and held after /RAS goes low.

2. /RAS has to go from high to low and remain low.

3. A column address has to be sent to address pins on the memory device for the specified amount of time and held after /CAS goes low.

4. /WE must be a logical high before /CAS transition. /WE must remain high until after the transition of /CAS.

5. /CAS has to switch from high to low and remain at a logic 0.

6. /OE must go low. Some systems allow /OE to cycle. /OE can also be tied to ground.

7. Data appears at the output pins. The time when the data appears depends on when /RAS and /CAS went low and when the address was applied.

8. Finally, /CAS and /RAS must return to their inactive states.
History of DRAM (Asynchronous)

- DRAM (Dynamic Random Access Memory)
- Invented in 1966 by Robert Dennard (IBM)
- MOS technology to simplify memory by controlling a capacitor
- Patent Issued in 1968
- Intel 1103 developed in 1970
  - 1K three-transistor design
History of DRAM (Asynchronous)

- Throughout the 70’s & 80’s the density of ram dramatically increased
- New modes to read/write
  - Fast Page Mode
  - Extended Data Out
  - Other burst type reads
History of DRAM (Synchronous)

- 1993 JEDEC Introduced the first SDRAM standard
- 1993 Samsung introduces KM48SL2000 SDRAM
  - Slower than previous DRAM
  - Clock controlled reading/writing
History of DRAM (DDR)

- 2000 JEDEC released DDR (Double Data Rate) Specification
  - Rising and falling edge of clock
  - Slower clock frequencies for better signal integrity
History of DRAM (DDR2)

- 2003 The first DDR2 memory module was released
- By the end of 2004, DDR2 was surpassing DDR
History of DRAM (DDR3)

- 2007 DDR3 first introduced
- Nearly doubled data transfer rate (up to 2133MT/s)
- ~30% less power consumption than DDR2
History of DRAM (DDR4)

- 2005 JEDEC began developing DDR4
- Scheduled to reach market by 2012
  - Failed to do so
  - Estimated to reach mass production by end of 2014
## DRAM Comparison Chart

<table>
<thead>
<tr>
<th>Feature/Option</th>
<th>DDR</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR4</th>
<th>DDR4 Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage (core and I/O)</td>
<td>2.5V-2.6V</td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
<td>Reduces memory power demand</td>
</tr>
<tr>
<td>Low voltage standard</td>
<td>No</td>
<td>Yes</td>
<td>Yes (DDR3L at 1.35V)</td>
<td>Anticipated (likely 1.05V)</td>
<td>Memory power reductions</td>
</tr>
<tr>
<td>Data rate (Mb/s)</td>
<td>333, 400, 667, 800</td>
<td>533, 667, 800, 1066</td>
<td>800, 1066, 1333, 1600, 1866, 2133</td>
<td>1600, 1866, 2133, 2400, 2667, 3200</td>
<td>Migration to higher-speed I/O</td>
</tr>
<tr>
<td>Densities</td>
<td>256Mb to 1Gb</td>
<td>256Mb to 4Gb</td>
<td>512Mb–8Gb</td>
<td>2Gb–16Gb</td>
<td>Better enablement for large-capacity memory subsystems</td>
</tr>
<tr>
<td>Internal banks</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>16</td>
<td>More banks</td>
</tr>
<tr>
<td>Bank groups (BG)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>Faster burst accesses</td>
</tr>
</tbody>
</table>
DDR4 Improvements

- Transfer Rate
- Data Integrity
- Power Consumption
- Memory Size
- Command Encoding
DDR4 Transfer Rate

- Support transfer rates of 2133MT/s up to 3200 MT/s
- Banks and Bank Groups
- Point-to-point topology
  - Single trace
- 284/288 pin DIMM
  - NVDIMM
DDR4 Transfer Rate
Number of banks is increased from 8 to 16.

DDR4 SDRAM architecture uses 8n prefetch with bank groups. This includes two or four selectable bank groups. This enables the DDR4 SDRAM to have separate activation, read, write or refresh operations underway in each of the unique bank groups. This technique increases the memory bandwidth and efficiency. It is particularly suited for memory applications where small levels of granularity are required.
There will no longer be a shared data bus for every 2 DIMMs.

Each DIMM will now have its own data bus.
DDR4 Data Integrity

- Parity Check for all commands and addresses
  - Enhanced recovery procedures
- Cyclic Redundancy Check on Data Bus CRC
  - Detect all 1 and 2-bit errors
  - ATM-8-HEC ($x^8+x^2+X+1$)
    - Same as GDDR4 and GDDR5
DDR4 Power

- Lower Voltage Requirement (1.2V)
- Data Bus Inversion
- Pseudo Open Drain
DDR4 Power

**DDR4 Data Bus Inversion (DBI)**

- Limit transistor switching by inverting/not inverting data
  - Extra bit added to data to signify inversion
- DBI-DC
  - Minimize number of ones/zeros transmitted
- DBI-AC
  - Compare current data with previous data
# DDR4 Data Bus Inversion (DBI)

<table>
<thead>
<tr>
<th></th>
<th>Controller</th>
<th>Data Bus</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ0</td>
<td>0 1 0 0</td>
<td>1 1 0 1</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>DQ1</td>
<td>1 1 0 0</td>
<td>0 1 0 1</td>
<td>1 1 0 0</td>
</tr>
<tr>
<td>DQ2</td>
<td>0 0 0 0</td>
<td>1 0 0 1</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>DQ3</td>
<td>0 1 1 0</td>
<td>1 1 1 1</td>
<td>0 1 1 0</td>
</tr>
<tr>
<td>DQ4</td>
<td>0 1 0 0</td>
<td>1 1 0 1</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>DQ5</td>
<td>1 0 1 0</td>
<td>1 1 1 1</td>
<td>1 0 1 0</td>
</tr>
<tr>
<td>DQ6</td>
<td>1 1 1 0</td>
<td>0 0 1 1</td>
<td>1 1 1 0</td>
</tr>
<tr>
<td>DQ7</td>
<td>0 0 1 0</td>
<td>1 0 1 1</td>
<td>0 0 1 0</td>
</tr>
</tbody>
</table>

Number of low bits: 5 3 4 8 4 3 4 1
DDR4 Power

Pseudo Open Drain

pseudo open drain I/O system

Data

Pseudo Open Drain (POD) interface of GDDR3/4

"High" No DC current

"Low" DC current

[SJ Bae. JSCC '08]
DDR4 Capacity

- Die Stacking
  - Reduced load (power)
  - Smaller footprint
- Smaller technology
New /ACT bit to replace old /RAS=L, /CAS=H, /WE=H combination and have larger row address range.
Future of Memory (DDR5?)

- Follows similar path while still viable
  - Increased speed
  - Higher density
  - Lower voltage
    - More focus here in coming future as mobile device market increases
Questions?