Intel Core Architecture

Stephen Moore
Overview

- NetBurst Microarchitecture
  - Pentium 4 Prescott
- Core Microarchitecture
  - Conroe and Merom
  - Wolfdale and Penryn
- Successor
  - Nehalem Microarchitecture
NetBurst Microarchitecture

- Released in 2000
- Created for High Clock Speeds
- 20 to 31 pipeline stages
  - Higher branch prediction miss penalty
- Heat problems
- Performance could not be scaled up
- 8 to 16 KB L1 cache
Pipeline

P5 Micro-Architecture

233MHz

P6 Micro-Architecture

Intro at
\[ \geq 1.4 \text{ GHz} \]

1 GHz
Today

.18\mu

Intel® NetBurst™ Micro-Architecture
Pentium 4 Prescott

- Single core
- 31 stage pipeline
- Expected 5 GHz clock frequency
- Achieved 3.6 GHz
- 2 MB L2 cache
- 90 nm transistor size
- 125 million transistors
- Max Thermal Design Power (TPD) of 103 W
## Benchmarks

### POVray 3.5

<table>
<thead>
<tr>
<th>Processor</th>
<th>PPS</th>
<th>Ranking</th>
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<tbody>
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### 3DMark03 Benchmark Results

<table>
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<th>Video Card</th>
<th>3DMarks</th>
<th>Ranking</th>
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Core Microarchitecture

- Released in 2006
- Multiple Cores
- Slower Clock
- Smaller Pipeline
- Halved TDP compared to Prescott
- 64 KB L1 cache
Conroe and Merom

- 2 cores
- Up to 14 stage pipeline
  - 4 instructions
- Max clock frequency of 3 GHz
- 4 MB L2 cache
- 65 nm transistor size
- 291 million transistors
- Max TDP of 65 W
Details

- 4 wide instruction decode
- 32 wide scheduler
- Out of order storage
- 128 bit packed instructions
- More performance, less power than previous design
L2 Cache

- 16 way
- 4 MB, 4096 lines
- Shared between cores
- 2.0ns delay from address-in to data-out
Cache Design

- L2 cache
  - 16 way
  - 4 MB, 4096 lines
  - Shared between cores
- Miss in L1
  - Checks other L1 and L2 in parallel
- 7 cycles from request to data return
- Larger L2 has longer delay times
- Competition for shared cache resources
Wolfdale and Penryn

- Released in 2007
- Die shrink
  - 45 nm transistor size
- Faster transistor switching
- Similar pipeline
  - New, faster divider hardware
- 410 million transistors
  - About 31 million per core
- 3 to 6 MB L2 cache
L2 Cache Design

- 6 MB cache size
- 24 way, 4096 lines
- Data is transferred as 64 bytes per line
- Organized as 1 MB slices
  - 4 way
  - 32 Data Banks
  - 8 Mid Logics
  - 4 Tag Banks
Benchmarks

Single-threaded performance

Multi-threaded performance

Memory-intensive applications

Overall performance

Thermal Design Power

- Intel Core 2 Duo E5300
- Intel Pentium 4 630
Nehalem Microarchitecture

- Released in 2008
- 4 to 8 cores
- 45 nm
- Reduced L2 Cache size
  - Unshared, 256 KB
- L3 cache shared by all cores
  - 4 to 12 MB
- Reintroduced Hyper-threading
- Kept smaller pipeline
Benchmarks

**CPU Mark Rating**

*As of 14th of May 2014 - Higher results represent better performance*

Intel Core i7 610 @ 2.53GHz - 1,989
Intel Core2 Duo E4500 @ 2.20GHz - 1,282
AMD Athlon 64 X2 Dual Core 4600+ - 1,200

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References