IBM POWER8 CPU

Nate Levesque, Kevin Alexandre
Outline

1. Background of POWER CPUs
2. POWER8
3. POWER8 vs POWER7
4. POWER vs other architectures
5. Future of POWER8
POWER Background
What is the POWER Architecture?

- RISC architecture developed by IBM
- Acronym for Performance Optimization with Enhanced RISC
- Not the same as POWER ISA (a deprecated IBM RISC architecture)
- Open for licensing
Timeline

1977: Research begins on POWER architecture
1980: First POWER prototype is completed
1990: POWER1
1991: POWERPC Created
1993: POWER2
1995: First 64bit POWER CPU
1998: POWER3
2001: POWER4
2004: POWER5
2007: POWER6 (Start of “modern” POWER era)
2010: POWER7
2013: POWER8

Credit: readwritethink.org timeline generator
Goals of POWER8

- Compete with the x86 Architecture
- Focus on support for Linux machines
- Create an open-source processor, with the OpenPOWER Consortium
- Scalability
- Target servers/large systems, IBMi OS’s, Linux
Implementations

- IBM’s Watson (POWER7-8)
- Mars rovers (POWER1)
- Servers
- PowerPC (modified version of POWER architecture)
POWER8 Introduction
Specifications

- 12 cores, 8 SMT each
- 2.5 to 5 GHz clock speed
- 650 millimeters square
- Binary compatible with previous POWER versions
- On-board power management based on the PowerPC 405 CPU
- Direct Integration of PCIe 3
CAPI: Coherent Accelerator Processor Interface

- Allows direct communication between CPU and PCIe connected devices
- Removes OS and Driver overhead
- More coherent memory addressing
- Follows more natural programming model
- Accomplished by circumventing I/O bridge used in predecessor
Coherent Accelerator Processor Interface (CAPI) Overview

Typical I/O Model Flow

Flow with a Coherent Model

Advantages of Coherent Attachment Over I/O Attachment

- Virtual Addressing & Data Caching
  - Shared Memory
  - Lower latency for highly referenced data

- Easier, Natural Programming Model
  - Traditional thread level programming
  - Long latency of I/O typically requires restructuring of application

- Enables Apps Not Possible on I/O
  - Pointer chasing, etc...

http://dancingdinosaur.wordpress.com/tag/coherent-accelerator-processor-interface-capi-power8/
Centaur

- Designed to be a generic memory controller
  - Memory can be upgraded from DDR3 to DDR4 when it is released
- Half L4 Cache, Half Controller
- Each POWER8 can have up to 8 Centaur Chips, 9.6 GB/s bandwidth per channel
POWER8 Memory Buffer Chip

...with 16MB of Cache...

Intelligence Moved into Memory
- Scheduling logic, caching structures
- Energy Mgmt, RAS decision point
  - Formerly on Processor
  - Moved to Memory Buffer

Processor Interface
- 9.6 GB/s high speed interface
- More robust RAS
- “On-the-fly” lane isolation/repair
- Extensible for innovation build-out

Performance Value
- End-to-end fastpath and data retry (latency)
- Cache → latency/bandwidth, partial updates
- Cache → write scheduling, prefetch, energy
- 22nm SOI for optimal performance / energy
- 15 metal levels (latency, bandwidth)
Pipeline

http://www.extremetech.com/computing/181102-ibm-power8-openpower-x86-server-monopoly
POWER8 Innovation

<table>
<thead>
<tr>
<th>Technology</th>
<th>POWER5 2004</th>
<th>POWER6 2007</th>
<th>POWER7 2010</th>
<th>POWER7+ 2012</th>
<th>POWER8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compute</td>
<td>130nm SOI</td>
<td>65nm SOI</td>
<td>45nm SOI eDRAM</td>
<td>32nm SOI eDRAM</td>
<td>22nm SOI eDRAM</td>
</tr>
<tr>
<td>Cores</td>
<td>2</td>
<td>2</td>
<td>8</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>Threads</td>
<td>SMT2</td>
<td>SMT2</td>
<td>SMT4</td>
<td>SMT4</td>
<td>SMT8</td>
</tr>
<tr>
<td>Caching</td>
<td>1.9MB</td>
<td>8MB</td>
<td>2 + 32MB</td>
<td>2 + 80MB</td>
<td>6 + 96MB</td>
</tr>
<tr>
<td>On-chip</td>
<td>36MB</td>
<td>32MB</td>
<td>None</td>
<td>None</td>
<td>128MB</td>
</tr>
<tr>
<td>Off-chip</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bandwidth</td>
<td>15GB/s</td>
<td>30GB/s</td>
<td>100GB/s</td>
<td>100GB/s</td>
<td>230GB/s</td>
</tr>
<tr>
<td>Sust. Mem.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak I/O</td>
<td>3GB/s</td>
<td>10GB/s</td>
<td>20GB/s</td>
<td>20GB/s</td>
<td>48GB/s</td>
</tr>
</tbody>
</table>
Comparison with Other Architectures
Benchmarks

http://www.hwsw.hu/kepek/hirek/2014/05/p8_spec1.jpg
POWER8 vs POWER7

- 2-3x faster
- CAPI
- Bigger caches and off-chip caching
- More cores and more threads
- Adds Centaur memory interconnects for higher memory bandwidth
POWER8 vs POWER7+

Socket Performance

POWER vs PowerPC
(Architecture)

- PowerPC is a modified version of POWER, with incompatibilities
  - PowerPC has some additional instructions
  - More restrictions on reserved fields in instructions
  - Different behaviour with reserved bits in registers
  - Others
POWER vs PowerPC (Target)

- PowerPC is basically a consumer version of POWER
POWER vs x86 Architecture

- Few differences in terms of general performance
- POWER is much better at virtualization
- POWER is better at data transaction processing and data analytics
Future of POWER8

- Expected to clock up to 5GHz over lifespan.
- Provide open-source alternative to x86.
- Overtake x86 as a more modern, more powerful platform.
Sources

- https://www.power.org/documentation/power-org-power-architecture-silicon-roadmap-update-2013/
- http://www.hwsw.hu/kepek/hirek/2014/05/p8_spec1.jpg
- http://www.extremetech.com/computing/181102-ibm-power8-openpower-x86-server-monopoly
Questions?