Agenda

- DDR SDRAM and Problems
- Solutions
- HMC
  - History
  - How it works
  - Specifications
- Comparisons
- Future
DDR

Diagram showing the structure of DDR Memory with components such as Row Buffer, Column Buffer, Control Circuitry, Data In/Out Buffers, Column Decoder, Sense Amps/Word Drivers, and Memory Array.
Problems

- DDR3:
  - Norm for average user
- DDR4:
  - Expensive
  - Less power (15W)
  - Around only 5% faster
  - Mostly for server farms
- GDDR5: (based on DDR2)
  - Expensive
  - Twice the bandwidth
  - Only in graphics cards
- Decreasing operating voltage
- Increasing # of banks
- Increase Frequency

Conclusion: Reaching limit of current technology
Solutions

- Wide I/O
- High-Bandwidth Memory (HBM)
- Hybrid Memory Cube (HMC)
Solutions – Wide I/O

- Layered Dram controlled with a logic layer
- Layers are linked with TSV
- Each Rank is a separate channel
- Each Channel contains a number of banks of data
- Hard to dissipate heat from DRAM layers
- Due to it’s 2.5D design, has great use in devices where size is important
Solutions – HBM

- HBM: High Bandwidth Memory
- Is like the ‘mid point’ between HMC and Wide I/O
- Four DRAM layers each divided into two channels
- TSV linked layers
- Hard to implement structure as currently proposed
HMC: History and Motivation

- Samsung and Micron decide that memory needed a new standard, away from DDR
- In order to make things easier to access, a vertical design is needed with excellent data accessibility
- In order to help the process, Micron and Samsung have started the Hybrid Memory Cube Consortium, a group comprised of over 100 companies
- First draft of the specifications was released August 14, 2012. Since then a revision 1.1 and 2.0 has been released.
- HBM, the Intel solution, is directly competing with HMC, the AMD solution
Through-Silicon Via (TSV)

- Allows stacking of semiconductors in layered fashion
- Allows for quick exchange of information between layers
- TSV extends from the PCB to the top layer of memory in HMC
- Critical Data paths are shorter, leading to better performance
- Is currently expensive to implement in Integrated Circuits
Hybrid Memory Cube (HMC)

- HMC contains multiple memory die and one logic base
- Memory Die and Logic Base contains multiple partitions
- A partition from each layer forms a Vault
- Each Vault is controlled by a Vault Controller
- Each Vault is completely independent
HMC: How it works – Structure

HMC Block Diagram

- Vaults are completely Independent
- Each vault completes its action out-of-order with its own timings
- Actions in vault are completed on a need basis
- Host Controller for HMC (after the external link) puts actions back in-order
Specifications – The Numbers

• 2 Configurations
  • 4GB, with 256 Banks
  • 8GB, with 512 Banks
• 320 GB/s Effective Bandwidth
• 70% less energy per bit than DDR3
• 90% less space than current RDIMMs
## Specifications – Data Packet

### Packets without Data

<table>
<thead>
<tr>
<th>Bit 127</th>
<th>64</th>
<th>63</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tail</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Header</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Packets with Data

(32B Data Payload Example)

<table>
<thead>
<tr>
<th>Flit #</th>
<th>Bit 127</th>
<th>64</th>
<th>63</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
</tr>
<tr>
<td>3</td>
<td>Tail</td>
<td>31</td>
<td></td>
<td>30</td>
</tr>
</tbody>
</table>

**Note:** Each numbered data field represents a byte with bit positions (7(MSB): 0(LSB)).

### Address Table

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte address</td>
<td>Bytes within the maximum supported block size</td>
<td>The four LSBs of the byte address are ignored for READ and WRITE requests (with the exception of BIT WRITE command; See BIT WRITE Command for details)</td>
</tr>
<tr>
<td>Vault address</td>
<td>Addresses vaults within the HMC</td>
<td>Lower three bits of the vault address specifies 1 of 8 vaults within the logic chip quadrant</td>
</tr>
<tr>
<td>Bank address</td>
<td>Addresses banks within a vault</td>
<td>Upper two bits of the vault address specifies 1 of 4 quadrants 4GB HMC: Addresses 1 of 8 banks in the vault 8GB HMC: Addresses 1 of 16 banks in the vault</td>
</tr>
<tr>
<td>DRAM address</td>
<td>Addresses DRAM rows and column within a bank</td>
<td>The vault controller breaks the DRAM address into row and column addresses, addressing 1Mb blocks of 16 bytes each</td>
</tr>
</tbody>
</table>
Specifications – Size and Layout

- Link
- GPIO
- Power grid

Note: 1. All dimensions are in millimeters.
# Comparisons

<table>
<thead>
<tr>
<th>Memory</th>
<th>DDR3/4</th>
<th>LPDDR3/4</th>
<th>Wide IOn</th>
<th>HMC</th>
<th>HBM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Applications</strong></td>
<td>PCs, laptops, servers, enterprise, consumer, embedded</td>
<td>Smartphones, feature phones, tablets, mobile electronics</td>
<td>High end smartphones</td>
<td>High end servers, high end enterprise</td>
<td>Graphics, computing</td>
</tr>
<tr>
<td><strong>JEDEC Standard</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>DRAM Interface</strong></td>
<td>Traditional parallel interface, single ended, bidirectional strobes, separate clock, etc.</td>
<td>Traditional parallel interface, single ended, bidirectional strobes, separate clock, etc.</td>
<td>Wide parallel interface. Signaling is similar to SDRAM. Wide IO is SDR, Wide IO2 is DDR.</td>
<td>Chip to chip SERDES interface.</td>
<td>Wide parallel, multi-channel interface. DDR signaling.</td>
</tr>
<tr>
<td><strong>Interface Voltage (V)</strong></td>
<td>DDR3: 1.5, 1.35, 1.25 DDR4: 1.2</td>
<td>LPDDR3: 1.2 LPDDR4: 1.1</td>
<td>Wide IO: 1.2 Wide IO2: 1.2</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td><strong>Interface Width (bits)</strong></td>
<td>4-72</td>
<td>16, 32, 64</td>
<td>Wide IO: 512 Wide IO2: 256, 512</td>
<td>Up to 4 links with up to 16 lanes each</td>
<td>128 per channel, up to 8 independent channels (1024 max)</td>
</tr>
<tr>
<td><strong>Max. Speed (Data Rate per pin in Mbps)</strong></td>
<td>DDR3 up to 2133 DDR4 up to 3200</td>
<td>LPDDR3 up to 2133 LPDDR4 up to 3200, possible plan to 4266</td>
<td>Wide IO up to 266 Wide IO2 up to 1066</td>
<td>10, 12.5 or 15 Gbps (SerDes)</td>
<td>Up to 2000</td>
</tr>
<tr>
<td><strong>Maximum Bandwidth (GBps)</strong></td>
<td>64-bit DDR3 up to 17 64-bit DDR4 up to 25.6</td>
<td>64-bit LPDDR3 up to 17 64-bit LPDDR4 up to 34</td>
<td>Wide IO up to 17 Wide IO2 up to 68</td>
<td>Up to 240</td>
<td>Up to 256</td>
</tr>
</tbody>
</table>
## Comparisons

<table>
<thead>
<tr>
<th></th>
<th>DDR3/4</th>
<th>LPDDR3/4</th>
<th>Wide IOn</th>
<th>HMC</th>
<th>HBM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>System Configuration</strong></td>
<td>Typically PCB based connections. Component &amp; DIMMs. SIP</td>
<td>Typically PoP point to point. Some PCB Connections via TSVs</td>
<td>DRAM stack on top of Apps Processor. Connection via TSVs</td>
<td>Point to point, short reach SERDES. PCB based</td>
<td>2.5D TSV based silicon interposer (SIP)</td>
</tr>
<tr>
<td><strong>Notable Features</strong></td>
<td>Familiar interface. No technical barriers, low risk</td>
<td>Familiar interface. No technical barriers, low risk</td>
<td>Relies on TSVs being mature. Mechanical stress, thermal, test, supply chain logistics may be complex.</td>
<td>Special logic die with memory controller at bottom of DRAM stack. Relies on TSVs being mature.</td>
<td>Relies on TSVs being mature. Mechanical stress, thermal, test</td>
</tr>
</tbody>
</table>
| **Benefits**  | • Mature infrastructure  
• Mature ecosystem  
• Low risk  
• Low cost | • Mature infrastructure  
• Mature ecosystem  
• Low risk  
• Low cost | • High bandwidth  
• Bandwidth scalability  
• Power efficiency  
• Compact footprint and form factor | • High bandwidth  
• Bandwidth scalability  
• Power efficiency  
• PCB connectivity between host and DRAM | • High bandwidth  
• Bandwidth scalability  
• Power efficiency |
| **Challenges** | • No longer scalable for speed  
• Signal integrity  
• Customers unprepared for integration challenges | • No longer scalable for speed  
• Signal integrity  
• Customers unprepared for integration challenges | • Relies on TSVs  
• Supply chain logistics (who does what and who is responsible for what)  
• Thermal and power delivery  
• Test and repair  
• Cost | • Relies on TSVs  
• Not a JEDEC standard  
• Cost  
• PHY IP infrastructure | • Relies on TSVs  
• Relies on 2.5D interposer  
• Cost  
• PHY IP infrastructure |
| **System Cost** | Lowest | Low | High | High | Modest |
Comparisons
The Future of HMC

- HMC aims to be the go-to technology for Servers and High-End Desktops
- Has been predicted to offer 400GB/s of bandwidth by developers in later iterations
- Expected to reach market in 2016, with commercial availability in early 2017
- Will replace DDR model of SDRAM, industry has agreed not to spend time evolving the DDR model
- Will break down the memory wall, and allow memory to be brought closer to Moore’s Law
Bibliography


The Shaaban smilies that missed the cut.
Questions?