BEAGLEBONE BLACK ARCHITECTURE

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MICHELLE ADVENA
AGENDA

- INTRO TO BEAGLEBONE BLACK
- HARDWARE & SPECS
- CORTEX-A8 ARMv7 PROCESSOR
- PROS & CONS
- VS RASPBERRY PI
- WHEN TO USE BEAGLEBONE BLACK
Single Board Computer
Low Cost
Small Size (Credit Card)
Community Supported

Open Sourced
(No Licenses Involved with BeagleBone materials)

Cortex-A8 ARM Processor from Texas Instruments

Simple to setup your own board (Linux comes installed)

Website: http://beagleboard.org/black
Wiki: http://elinux.org/Beagleboard:BeagleBoneBlack
BeagleBone Black
1 GHz performance ready to use for $45

10/100 Ethernet

USB Host
Easily connects to almost any everyday device such as mouse or keyboard

microHDMI
Connect directly to monitors and TVs

Serial Debug

DC Power

Power Button

LEDS

Reset Button

USB Client
Development interface and directly powers board from PC

microSD
Expansion slot for additional storage

512MB DDR3
Faster, lower power RAM for enhanced user-friendly experience

Expansion headers
Enable cape hardware and include:
- 65 digital I/O
- 7 analog
- 4 serial
- 2 SPI
- 2 I2C
- 8 PWMs
- 4 timers
- And much much more!

1 GHz Sitara AM335x ARM® Cortex™-A8 processor
Provides a more advanced user interface and up to 150% better performance than ARM11

2GB on-board storage using eMMC
- Pre-loaded with Ångström Linux Distribution
- 8-bit bus accelerates performance
- Frees the microSD slot to be used for additional storage for a less expensive solution than SD cards

Included in price:
- Power supply ~ $10
- USB network cable ~ $3
- 2GB on-board storage $5-10
- PRU for real-time tasks typically on FPGA ~ $20

SPECS

AM335x 1GHz ARM® Cortex-A8 Processor
512MB DDR3 RAM
4GB 8-bit eMMC on-board flash storage
3D graphics accelerator
NEON floating-point accelerator
2x PRU 32-bit microcontrollers

Latest: Rev C
<table>
<thead>
<tr>
<th>Cortex-A8 Technologies</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TrustZone Security</td>
<td>Device Integrity / Secure Transactions</td>
</tr>
<tr>
<td>Jazelle RCT Acceleration / Thumb 2EE Instruction Set</td>
<td>Fast &amp; Responsive Java Applications</td>
</tr>
<tr>
<td>Thumb-2 Instruction Set</td>
<td>Greater Performance With Less Code Size</td>
</tr>
<tr>
<td>NEON™ Advanced SIMD(+VFPv3)</td>
<td>Enhanced Multimedia Experience</td>
</tr>
<tr>
<td>Superscalar ARMv7 Core</td>
<td>Highest-performance mobile processor</td>
</tr>
</tbody>
</table>

**NEON**

★ SIMD (Single Instruction Multiple Data) accelerator processor

★ 64/128-bit Hybrid SIMD architecture

★ single instruction performs the same operation on multiple elements that are packed within registers

★ Parallel architecture

★ Two Integer 64-bit ALUs

★ Fully pipelined

NEON

❖ Two Integer 64-bit ALUs operating in parallel
  ➢ Can perform 128-bit length equivalent ALU operation in 1 cycle
❖ Supports 128-bit data streaming from both L1D$ and L2$
  ➢ Byte permute function allows for on-the-fly data shuffling
❖ Two Integer Multipliers of 32x16
  ➢ Each can perform one 32x16, two 16x16 or four 8x8 operations in a single pass
  ➢ Support 32x32 operation in two passes

Native support for structures (e.g. complex numbers, pixels, coordinates)

Memory treated as an array of structures (AoS)

Eliminates ‘shuffling’ overhead

- Optimised memory access as single transfer
- Data arranged for efficient SIMD processing

BENEFITS OF NEON

+ both aligned and unaligned data access
  + efficient vectorization of SIMD operations
+ both Integer and FP
  + broader range of applications (compression decoding, 3D graphics)
+ tightly coupled to ARM core
  + single instruction stream & unified view of memory
    + single development platform target
    + simpler tool flow
+ large register file with multiple views
  + efficient handling of data & minimizes memory accesses
    + better throughput performance
HIGH-LEVEL BLOCK DIAGRAM

[Diagram showing the block diagram of a system with various components like ARM Cortex-A8, Graphics, Display, PRU-ICSS, Serial, System, Parallel, Memory interface, etc.]

Figure 3-1. Microprocessor Unit (MPU) Subsystem

- MPU Subsystem
- OCP2 ATB
- Cortex A8
- L1 I 32KB w/SED
- L1 D 32KB w/SED
- ETMSOC
- Debug Bus (OCP)
- System Interrupts
- AXI2OCP 275 MHz
- AINTC 275 MHz
- ROM 176 KB
- OCM RAM (SRAM internal) 64 KB
- I2ASYNC 550 MHz
- MPU PLL
- CLK_M_OSC Frm Master OSC
- T2ASYNC 200 MHz
- To L3
- OCP Master 0
- OCP Master 1
- To L3
- I2ASYNC 550 MHz
- 64
- 128
- 64
- 32

http://www.ti.com/lit/ug/spruh73l/spruh73l.pdf
ARM CORTEX-A8 MPU SUBSYSTEM

ARMv7 and Thumb 2 ISA

ISA Efficiency = 2.01 DMIPS/MHz

dual-issue, in-order execution engine

Integrated L1 and L2 caches with NEON™ SIMD (Single Instruction, Multiple Data) Media Processing Unit

Static Scheduling with Instruction Replay on Memory Stall

Fire-And-Forget Issue
CACHE

- **Split Level 1 Caches - Instruction and Data**
  - Both 16 kB
  - 4-way Set Associative
  - Single Cycle Load-Use Penalty

- **Unified Level 2 Cache**
  - 256 kB
  - 8-Way Set Associative
  - Minimum Latency - 8 Cycles
  - High BW Interface to L1 Cache
MEMORY: GPMC

Fully pipelined
Onboard flash: 4GB, 8-bit
embedded MMC
SDRAM Mem: 512MB DDR3L
800MHz
PIPELINE
dual-issue, in-order
95% Accuracy in Dynamic Branch Prediction

Dynamic branch predictor components

- 512-entry 2-way BTB
- 4K-entry GHB indexed by branch history and PC
- 8-entry return stack

Branch resolution

- resolved in single stage
- maintains speculative and non-speculative versions of branch history and return stack
INSTRUCTION DECODE

4 entry pending queue
➔ decreases fetch stalls
➔ increases pairing opportunities

**replay queue**: keeps instructions for reissue on memory system stall

**scoreboard**: static scheduling to predict register availability
cross-checks in D3 allow issue of dependent instruction pairs
- 2 symmetric ALU pipelines: Shift/ALU/SAT
- Load/store pipe used by instructions in either pipeline
- Multiply instructions are tied to pipe 0
- All key forwarding paths supported
- Static scheduling allows for extensive clock gating
NEON PIPELINE

❖ Instruction issue
  ➢ static scheduling with fire-and-forget issue
  ➢ 1 LS + 1 NINT/NFP can issue each cycle

❖ Execution pipelines
  ➢ All pipelines are 64-bit SIMD
  ➢ Floating-point MAC executed using both FADD and FMUL pipelines
NEON: INTERFACING
NEON

16-Entry Instruction queue

Dual view register file

- 32 x 64-bit
- 16 x 128-bit

6 Stage execution Pipeline

- Integer
- Single precision floating point

Load store permute

Non-pipelined IEEE vector floating point support

12-Entry load data queue
PRU-ICSS

Programmable Real Time Unit Subsystem and
Industrial Communication Subsystem

Dual PRUs

Three 120-byte register banks accessible by each

Supports e.g. EtherCAT, PROFIBUS, PROFINET, EtherNet/IP

12KB of Shared RAM With Single-Error Detection (Parity)

UART port

eCAP module

Dual MII Ethernet Ports

Single NDIO Port

http://www.ti.com/lit/ug/spruh73l/spruh73l.pdf
## POWER

**TPS65217C PMIC regulator + LDO**

<table>
<thead>
<tr>
<th></th>
<th>TPS65217x</th>
<th>TPS65910x</th>
<th>TPS650250</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Battery Charger</strong></td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>Boost</strong></td>
<td>WLED backlighting</td>
<td>5V Boost</td>
<td>No</td>
</tr>
<tr>
<td><strong>AM335x OPP</strong></td>
<td>OPP50, OPP100</td>
<td>OPP50, OPP100, OPP120, Turbo, Nitro</td>
<td>OPP50, OPP100, OPP120, Turbo, Nitro</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>3 DCDC @ 1.2A, 4 LDO</td>
<td>2 DCDC @ 1.5A, 1 DCDC @ 1A, 9 LDO</td>
<td>1 DCDC @ 1.6A, 2 DCDC @ 0.8A, 3 LDO</td>
</tr>
<tr>
<td><strong>Input Voltage Range</strong></td>
<td>2.7 - 5.8 V</td>
<td>2.7 - 5.5 V</td>
<td>2.5 - 6.5 V</td>
</tr>
<tr>
<td><strong>DVFS / SmartReflex</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>RTC-only mode</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>DDR</strong></td>
<td>DDR2, LPDDR1</td>
<td>DDR3</td>
<td>DDR2, LPDDR1, DDR3</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>48pin QFN, 6mm x 6mm</td>
<td>48pin QFN, 6mm x 6mm</td>
<td>32pin QFN, 5mm x 5mm</td>
</tr>
<tr>
<td><strong>T&lt;sub&gt;A&lt;/sub&gt;</strong></td>
<td>-40°C to 105°C</td>
<td>-40°C to 85°C</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td></td>
<td>BeagleBone Black</td>
<td>Raspberry Pi</td>
<td></td>
</tr>
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<td>------------------------</td>
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<tr>
<td><strong>Base Cost</strong></td>
<td>$45</td>
<td>$35</td>
<td></td>
</tr>
<tr>
<td><strong>Processor Speed</strong></td>
<td>1 GHz</td>
<td>700 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>GPIO</strong></td>
<td>65 pins</td>
<td>8 pins</td>
<td></td>
</tr>
<tr>
<td><strong>Power Consumption</strong></td>
<td>210-460 mA @ 5V</td>
<td>260-350 mA @ 5V</td>
<td></td>
</tr>
<tr>
<td><strong>Onboard Storage</strong></td>
<td>4 GB, SD</td>
<td>SD card</td>
<td></td>
</tr>
<tr>
<td><strong>Cache</strong></td>
<td>L1 - 32 kB</td>
<td>L1 - 16 kB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L2 - 256 kB</td>
<td>L2 - 128 kB</td>
<td></td>
</tr>
<tr>
<td><strong>ISA Efficiency</strong></td>
<td>2.01 DMIPS/MHz</td>
<td>1.25 DMIPS/MHz</td>
<td></td>
</tr>
<tr>
<td><strong>RAM</strong></td>
<td>512 MB DDR3L</td>
<td>512 MB SDRAM</td>
<td></td>
</tr>
<tr>
<td><strong>Video Connections</strong></td>
<td>Micro HDMI</td>
<td>HDMI, Composite</td>
<td></td>
</tr>
<tr>
<td><strong>Audio Connections</strong></td>
<td>HDMI</td>
<td>HDMI, 3.5 mm Jack</td>
<td></td>
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</tbody>
</table>
WHEN TO USE THE BEAGLEBONE BLACK...

- Processing Speed is important
- Constrained Size Requirements
- Projects with Many Hardware Connections
- Projects that may be commercialized
  - Open Sourced
- Non-Media Heavy Projects
  - Raspberry Pi is a slightly better option here
- Simple Startup
  - Linux Distro already installed
REFERENCE

AM335x Sitara Processors Technical Reference Manual (Rev. L)
http://www.ti.com/lit/ug/spruh73l/spruh73l.pdf

AM335x Sitara™ Processors (Rev. H)

NEON & VFP

Cortex A8 Arch
http://processors.wiki.ti.com/index.php/Cortex-A8_Architecture

A8 NEON Arch

logo (w/ raspi) from
http://www.itclips.net/wp-content/plugins/rss-poster/cache/ef657_bbvrpi-e1374615365689.png

logo (larger, w/ wifi) from
https://fleshandmachines.files.wordpress.com/2012/07/beagle.png
QUESTIONS?