Evolution of ARM Processor Architecture

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ARM History

- **Advanced RISC Machine**
- 1979 – Acorn Computers Created
- 1985 – first RISC processor (ARM1)
  - 25,000 transistors
  - 32-bit instruction set
  - 16 general purpose registers
  - Load/Store Multiple Instructions
  - 26-bit address space
- November 2010 – Advanced RISC Machines Ltd
  - Create base tech. and license intellectual property
- Currently most widely used architecture in the world
Over 700 Licenses
## Architecture Versions

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<td>ARMv8</td>
<td>No cores available yet. Will support 64-bit data and addressing</td>
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ARMv2

- ARM2 – 1986
  - 30,000 transistors
  - 32-bit data bus
  - 26-bit address bus
  - Acorn “Archimedes” (1987)
  - Not successful

- ARM3 – 1990
  - Instruction cache added
  - Clock rate increased to 25 MHz
ARMv3

- ARM6, ARM7
  - ARM6 no longer used
- 32-bit addressing
- Long multiply support
- 3 stage pipeline
  - Fetch, decode, execute
- ARM4 and ARM5?
ARMv4

- 1994 – ARM7 first well-known processor
- First architecture used in mobile devices
- ARM7, ARM9 still used
- ARM9 vs. ARM7
  - Harvard Architecture
  - DSP Functionality
- StrongARM – 1996
  - Acquired by Intel – 1997
- Added Halfword load and store instructions
- Thumb state
ARMv4 (cont.)

- Thumb Instructions
  - 16-bit instructions
  - Code Density
  - Decompressed in Decode
  - Less Functionality
ARMv5

- ARM7, ARM9 still have licenses
  - ARM9 used in first smartphones
  - ARM9 best selling ARM processor family
- Xscale – Intel and Marvells (2002)
  - StrongARM successor
  - No floating point operations
  - Superpipelined Microarchitecture
- Improved ARM and Thumb interworking
  - Quickly and easily switch between the two
ARMv5 (cont.)

- Jazelle
  - Third execution mode to execute Java bytecode
  - Low memory when switching tasks
- Enhanced DSP Instructions
  - 16-bit Multiply Operations
  - Count leading-zeroes instruction
- 5 stage pipeline
  - Fetch, decode, execute, memory, writeback
  - Most instructions now performed in one cycle
ARMv6

- ARM11 is still used today in many smartphones
- Beginning of Cortex–M series of processors
- Improved memory management
  - Improved by over 30%
  - More efficient bus usage, direct memory access, reduced average instruction fetch and data latency, physically tagged cache
- Multimedia support
  - Over 60 Single Instruction Multiple Data Capabilities
  - Sum of Absolute Differences instruction improved by 15 cycles
ARMv6 (cont.)

- Multiprocessing
  - Improved sharing memory between processors and synchronizing them
  - Load/store exclusive instructions with semaphores

- Improved data handling
  - System on a chip integration leads to the system being mixed-endian
  - E-bit set and cleared using SETEND
  - Byte reverse instructions to transform endianness of data

- 8 stage single-issue pipeline
  - Hardware branch prediction
  - Split Instruction/Data Level1 caches physically tagged
  - Out of order completion
ARMv7

- Cortex-A: Applications  
  - Internet access, media, graphics
- Cortex-M: Microcontrollers  
  - Low energy, longer battery life
- Cortex-R: Real-time Devices  
  - Reliable, error correction, parity checks
- NEON  
  - 10-stage pipeline  
  - Dual issue, in order execution  
  - 2 cache levels, split and unified  
  - General-purpose SIMD engine – great for media
ARMv7 (cont.)

- Jazelle–RCT
  - Ahead-of-time compilation
  - Just-in-time compilation

- Thumb–2
  - Minimizes code density
  - Given new instructions

- Floating Point Architecture
  - Now tightly coupled with CPU
  - Half, single, double precision floating point ops
  - Thumb and ThumbEE can now also run
ARMv7 (cont.)

- **TrustZone**
  - Integrated in Cortex-A processors
  - Protects memory, keyboards, screens from attacks
  - Hardware and software partitioned into subsystems
  - One processor for both subsystems
  - 3 levels of implementation
    - Secure OS for payment on device
    - Digital Rights Management
    - Authorization of viewing materials with keys

- **SecurCore**
  - Secure solutions for smart cards
  - Used by TrustZone
Normal world

- Normal world user mode
- Normal world privileged modes

Secure world

- Secure world user mode
- Secure world privileged modes

Monitor mode
ARMv7 (cont.)

- big.Little Processing
  - Way to extend battery life up to 70%
  - “big” processor: Cortex-A15
    - Big performance
  - “Little” processor: Cortex-A7
    - Little energy
  - When a device has high workloads, can switch to A15 for maximum performance, otherwise stays with low energy processor
Cortex-A15 Processor

- 2.5 GHz
- Virtualization
  - Migrate OS instances between servers quickly
  - Run multiple OS instances simultaneously on CPU
- Large Physical Address Extension
  - 32-bit virtual memory addresses can be mapped into 40-bit physical address spaces
  - New page table format
  - Physical address space can be 4 kB
- 12 stage pipeline
  - 1 12-stage in order, 3 12-stage out of order
ARMv8

- 64-bit architecture
- 30 general purpose registers
  - 64 bits wide
- Load–acquire/Store–release instructions
  - Higher performance in concurrent programs
- Instruction level support for cryptography
  - 2 encode and decode instructions
- Large Physical Address Extensions
  - 48-bit physical addresses
  - Page table down to 4 levels
- Backwards compatibility
Revenue & Market Share

- 6.1 Billion chips sold in 2010
  - 55% increase from 2009
- Highly used in mobile and embedded devices
  - 95% of smartphones
  - 10% of mobile computers
  - 35% digital TV and STB
- $192 million revenue – 2011 third quarter
  - 22% increase from 2010
What’s Next?

- Windows 8
  - OS for many different devices
  - 23% of PCs by 2015
- ARMv8
  - Largest architectural change in ARM’s history
  - Release of Armv8 prototype products in 2014
- Extending to server markets
  - HP productions – 2012
- Continue to be the most widely used architecture
References

Questions?