TMS320C6678 Multicore DSP

Avery Francois & Brian Koziel
Overview

- Motivation
- TMS320C6678 Overview
- KeyStone Architecture
  - Multicore Navigator
  - Memory
  - TeraNet
  - HyperLink
- Applications
- Benchmark Comparisons
Motivation

- Efficient implementation of algorithms on digital signals
- Process digitized data streams
- Meet real-time and power constraints
History

- First Generation (early 1980’s)
  - Simple architectures, 1 MAC
- Second Generation (late 1980’s)
  - Complex instructions, 1 MAC
- Third Generation (early 1990’s)
  - Parallel execution unit: SIMD, >1 MAC
- Fourth Generation (late 1990’s)
  - VLIW, Superscalar
- Fifth Generation (2010’s)
  - Multi-core VLIW
TI’s History

1930 - Started out as a small oil and gas company
1946 - Applied signal processing technology for submarine technology and radar, creating an electronics equipment lab and manufacturing unit
1954 - Invented the silicon transistor and changed name to Texas Instruments Incorporated
1967 - Created the first electronic handheld calculator
1983 - Created its first single-chip DSP (TMS32010)
1990s and 2000s - Expanded to cell phone embedded processing elements
2011 - Acquired National Semiconductor
TI’s Vision

- Provide analog and embedded processing solutions for a better world
- TI’s technology is used in virtually every industry
- Hold over 40,000 patents
- 70% of products are produced, assembled, and tested internally
Texas Instrument Product Lines

- **C5000 series**
  - Ultra low power devices
  - All fixed point processors
- **C6000 series**
  - Power optimized
  - Multicore fixed and floating point
- **DaVinci Video Processors**
  - Video processing SoC
  - Media processors for Industrial video and imaging
Texas Instrument Product Lines

- Keystone Multicore Architecture
  - Multicore DSPs
    - C665x series
    - C667x series -> (C6678)
  - Multicore DSPs + ARM processors
    - Embedded platforms
    - High performance computing
    - FPGA alternative platforms
## Key Features

- 8 DSP cores
- 1.0 GHz - 1.4 GHz
  - Fixed and floating point
  - 22.4 GFLOP/Core @ 1.4 GHz
- 64 kB L1 cache per core
- 512 kB L2 cache per core
- Multicore Navigator
- Network Coprocessor
  - Packet Accelerator
  - Security Accelerator

**TMS320C6678**

$272
Peripherals

- Four lanes of SRIO
- PCIe Gen2
- HyperLink
- Gigabit Ethernet
- 64-bit DDR3 interface
- 16-bit EMIF
- Two telecom serial ports
- UART
- I²C
- 16 GPIO Pins
- SPI Interface
- Semaphore Module
- Sixteen 64-bit Timers
- Three on-chip PLLs

TMS320C6678
KeyStone Architecture

5 generations of multicore
- Lowers development effort
- Speeds time to market
- Leverages TI's investment
- Optimal software reuse

- C64x+ Fixed Point Only
- C64x Single core DSP
- C66x Fixed AND floating point DSP
- Networking + Wireless Acceleration
- 32 bit ARM A15
- 10G Networking
- 64 bit ARM v8
- C66x+ DSP
- 40G Networking

KeyStone Architecture

- Multi-core DSP architecture
- Multi-core Navigator
- Memory Structure
- Teranet
- HyperLink
- Coprocessors
- Debug
Overall Design
Multicore Navigator

- “Fire and Forget” inter-core communications
- Low-overhead processing and routing of packet traffic
- Dynamic load optimization
- Designed to minimize host interaction, while maximizing memory and bus efficiency
- Queue Manager Subsystem (QMSS)
- Dedicated packet DMA (PKTDMA) engines
Multicore Navigator
Overall Design
Memory Structure

- **Called “CorePac”**
  - 32KB level-1 program memory (L1P)
  - 32KB level-1 data memory (L1D)
  - 512KB level-2 memory (L2)
  - 4096KB multicore shared memory (MSM)
  - All memory on the C6678 has a unique location in the memory map
Memory Structure Cont.

MSM SRAM is a configurable memory section
- Memory size is 4096KB
- Can be configured as shared L2 and/or shared L3 memory
- Allows extension of external addresses from 2GB to up to 8GB
- Has built in memory protection features
Memory Protection

The operating system defines who or what is authorized to access the L1D, L1P, and L2 memory on a per page level.

- 16 pages of L1P (2KB each)
- 16 pages of L1D (2KB each)
- 32 pages of L2 (16KB each)

The DSP and each of the system masters on the device are all assigned a privilege ID. It is possible to specify whether memory pages are locally or globally accessible.
Memory Protection Cont.

- A page may be marked as either (or both) locally accessible or globally accessible.
- A DSP or DMA access to a page without the proper permissions will
  - Block the access — reads return 0, writes are ignored
  - Capture the initiator in a status register — ID, address, and access type are stored
  - Signal event to DSP interrupt controller

<table>
<thead>
<tr>
<th>AIDx Bit</th>
<th>Local Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>No access to memory page is permitted.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Only direct access by DSP is permitted.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Only accesses by system masters and IDMA are permitted (includes EDMA and IDMA accesses initiated by the DSP).</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>All accesses permitted.</td>
</tr>
</tbody>
</table>
Overall Design
All system peripherals, CorePacs, and controllers are interconnected through the “TeraNet”. TeraNet is a non-blocking switch fabric enabling fast and contention-free internal data movement. Every connected device is classified as either a master or slave.

- Configuration Buses: Used to access the register space of a peripheral.
- Data Buses: Mainly for data transfers.
HyperLink Interconnect

- Provides a 50-Gbaud chip-level interconnect that allows SoCs to work in tandem.
- Has a low-protocol overhead and high throughput making it an ideal interface for chip-to-chip communication.
- Works with the Multicore Navigator by dispatching tasks to tandem devices transparently and executing tasks as if they are running on local resources.
Applications

The C6678 is the most powerful stand alone multi-core DSP TI has to offer, enabling its use in a wide range of applications throughout industry.

- **Defense**: radar processing, munitions & targeting, and avionics.
- **Machine Vision**: mixed precision algorithms and controls processing.
- **Medical Imaging**: ultrasound, surgical x-ray, optical coherence tomography, and MRI systems.
- **Multimedia Infrastructure**: media gateways, IMS servers, cable head-end equipment, and video broadcasting.
- **Test and Automation**: real world signals such as vibration, acoustics, electrical properties, radio frequencies, image and video data.
## Keystone Family Comparison

<table>
<thead>
<tr>
<th>SubFamily</th>
<th>CPU</th>
<th>Frequency (MHz)</th>
<th>Peak MMACS</th>
<th>External Memory Type Supported</th>
<th>On-Chip L1/SRAM</th>
<th>On-Chip L2/SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMS320C6654 - Fixed and Floating Point Digital Signal Processor</td>
<td>C665x DSP</td>
<td>1 C66x</td>
<td>850</td>
<td>DDR3 1066 SDRAM</td>
<td>64 KB (32 KB Data, 32 KB Program per core)</td>
<td>1024 KB (0 KB Shared)</td>
</tr>
<tr>
<td>TMS320C6655 - Fixed and Floating Point Digital Signal Processor</td>
<td>C665x DSP</td>
<td>1 C66x</td>
<td>1000 1250</td>
<td>DDR3 1333 SDRAM</td>
<td>128 KB (32 KB Data, 32 KB Program per core)</td>
<td>2048 KB (1024 KB Shared)</td>
</tr>
<tr>
<td>TMS320C6656 - Fixed and Floating Point Digital Signal Processor</td>
<td>C665x DSP</td>
<td>2 C66x</td>
<td>1000 1250</td>
<td>DDR3 1333 SDRAM</td>
<td>128 KB (32 KB Data, 32 KB Program per core)</td>
<td>3072 KB (1024 KB Shared)</td>
</tr>
<tr>
<td>SM320C6678; HIREL; Multicore Fixed and Floating-Point Digital Signal Processor</td>
<td>C667x DSP</td>
<td>8 C66x</td>
<td>1000</td>
<td>DDR3 1600 SDRAM</td>
<td>512 KB (32 KB Data, 32 KB Program per core)</td>
<td>8192 KB (4096 KB Shared)</td>
</tr>
<tr>
<td>TMS320C6670 - Multicore Fixed and Floating-Point System-on-Chip</td>
<td>C667x DSP</td>
<td>4 C66x</td>
<td>1000 1200</td>
<td>DDR3 1600 SDRAM</td>
<td>256 KB (32 KB Data, 32 KB Program per core)</td>
<td>6144 KB (2048 KB Shared)</td>
</tr>
<tr>
<td>TMS320C6671 - Fixed and Floating-Point Digital Signal Processor</td>
<td>C667x DSP</td>
<td>1 C66x</td>
<td>1000 1200</td>
<td>DDR3 1600 SDRAM</td>
<td>64 KB (32 KB Data, 32 KB Program)</td>
<td>4608 KB (4096 KB Shared)</td>
</tr>
<tr>
<td>TMS320C6672 - Multicore Fixed and Floating-Point Digital Signal Processor</td>
<td>C667x DSP</td>
<td>2 C66x</td>
<td>1000 1250 1500</td>
<td>DDR3 1600 SDRAM</td>
<td>128 KB (32 KB Data, 32 KB Program per core)</td>
<td>5120 KB (4096 KB Shared)</td>
</tr>
<tr>
<td>TMS320C6674 - Multicore Fixed and Floating-Point Digital Signal Processor</td>
<td>C667x DSP</td>
<td>4 C66x</td>
<td>1000 1250</td>
<td>DDR3 1600 SDRAM</td>
<td>256 KB (32 KB Data, 32 KB Program per core)</td>
<td>6144 KB (4096 KB Shared)</td>
</tr>
<tr>
<td>TMS320C6678 - Multicore Fixed and Floating-Point Digital Signal Processor</td>
<td>C667x DSP</td>
<td>8 C66x</td>
<td>1000 1250</td>
<td>DDR3 1600 SDRAM</td>
<td>512 KB (32 KB Data, 32 KB Program per core)</td>
<td>8192 KB (4096 KB Shared)</td>
</tr>
</tbody>
</table>
Single Core Comparison

Fixed Point Comparison
Works Cited


Questions