XILINX Zynq 7000
All Programmable SoC
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Outline

- What is the benefit?
- Brief History
- Hardware Overview
  - Product Line
  - Processing System
  - Programmable Logic
- Development Environment
- High level Synthesis
- Performance Comparisons
What is the benefit?

- **General Purpose Processors (GPPs)**
  - Good at handling a workload that is unknown
  - Generally bad application specific performance

- **Reconfigurable Computing**
  - Provides faster time to market and cheaper cost than ASICs
  - Allows hardware acceleration of software applications
  - Does not have the benefit of GPP generality (can have soft-core processors, but these are not as effective as standard hard-core processors)

- **Application Specific Processors (ASPs)**
  - Tailored to specific application, so faster operation than GPP on those tasks
  - Changes in domain require new ASP to be made.... expensive

- **Why not have it all?**
Xilinx Timeline

- **Founded (1984)**
- **First HLS Tools (2004)**
- **AutoESL AutoPilot (2009)**
- **Zynq 7000 (2011)**
- **Vivado HLS (2012)**

**1985**
- XC2000 Series
- 1.2k gates
- 64 CLBs

**1998**
- Virtex Series
- 1M gates
- 384 CLBs

**2009**
- Virtex6 Series
- 12M gates
- 60k CLBs

**2012**
- Virtex7 Series
- 30M gates
- 300k CLBs
Product Overview

- 7 Chips across 2 families
Processing System (PS)

- ARM Cores
- On-Chip memory
- Off-Chip memory
- DMA Controller
- I/O (IEEE, Ethernet, USB2, SPI, UART, I2C, CAN2A/B)

Programmable Logic (PS)

- Configurable logic blocks (CLB)
- DSP Blocks
- Programmable I/O
- JTAG
- PCI-E 8x
- Serial Transceivers
- 12-bit Analog to Digital Converters
ARM Cortex A9

- Dual Core 32bit
- Up to 1 GHz
- 32KB L1 Cache
- 512 L2 Cache
- 256 KB on-chip RAM
- 16/32bit interfaces for DDR3 or DDR2
- 8 Channel DMA controller (direct memory access) Mem-Mem, Mem-Peripheral, Peripheral-Mem
Programmable Logic

Artix-7 FPGAs

- 28k - 85k Logic Cells
- 17,600 - 53,200 LUTS
- 35,200 - 106,400 Flip Flops
- 60*240KB - 140*560KB Block RAM
- Peak DSP Performance
  - 100 - 276 GMACs (Sym. FIR)

Kintex-7 FPGAs

- 125k - 444k Logic Cells
- 78,600 - 277,400 LUTS
- 157,200 - 554,800 Flip Flops
- 265*1,060 KB - 755*3020KB Block RAM
- Peak DSP Performance
  - 400 - 2020 GMACs (Sym. FIR)
Interface between APU and FPGA

- AXI Protocol
  - Developed by ARM
  - Defines a set protocol that allows reuse of IP cores
  - Tailored to large data transfers
  - Tightly coupling between FPGA and APU resources

- Faster communication is required to be able to take full advantage of the FPGA speedups
Vivado Design Environment
Development Environment
Development Environment
High Level Synthesis
High Level Synthesis

- Create hardware automatically (sort of)
  - Interconnects between FPGA fabric and processor are figured out for you. As simple as writing data to a register
  - Supports C, C++ and System C
    - but it can't do better than an engineer can it...? (don't take my job!)
    - It does surprisingly well...
- Personal testing
  - AES 128 bit algorithm custom made algorithm to be ran in 11 clock cycles (time to complete 1 week)
  - AES 128-bit algorithm using a posted online C implementation - 19 clock cycles (time to complete 20 min)
  - Keccak algorithm custom implementation - 24 clock cycles - 2 weeks
  - Keccak in HLS - ~10000?? clock cycles - 1 hour
Basic Idea

From any C code example...

Operations are extracted...

The control is known

A unified control dataflow behavior is created.
void foo(int in[3], char a, char b, char c, int out[3]) {
    int x, y;
    for(int i = 0; i < 3; i++) {
        x = in[i];
        y = a*x + b + c;
        out[i] = y;
    }
}
Performance Metrics

- Who’s Cortex reigns supreme
  - Benchmark tests embedded system CPU’s with typical embedded workloads
Performance Metrics - Power

-1LI and -2LI shown below deliver average savings of 20% total power

SDR  Motor Control  Driver Assistance  Surveillance  Factory Automation

Total Power (Watts)

Ynq®-7000 Z-7020 vs. Cyclone V SoC 5CSXFG6C
Ynq®-7000 Z-7010 vs. Cyclone V SoC 5CSXFG6C
Ynq®-7000 Z-7020 vs. Cyclone V SoC 5CSXFG6C
Ynq®-7000 Z-7020 vs. Cyclone V SoC 5CSXFG6C
Ynq®-7000 Z-7030 vs. Cyclone V SoC 5CSXFG6C
Ynq®-7000 Z-7030 vs. 2x Stratix V FPGAs
Future of SoC (Xilinx UltraScale)

- Quad Core Cortex A53 with Dual-Arm Cortex R5 coprocessors
- ARM Mali™-400MP Graphics Processor
- H.265/264 Video Codec Unit
- Configuration Security Unit
- DDR 4 support
- New development environment to allow CPU/FPGA/GPU implementation with minimal knowledge of each system
Our conclusions

- System-on-chip solution that leverages many different design styles (FPGA, ASP, GPP, GPU) all on chip
- Design tools that allow use of all elements without need for full understanding how things are connected
  - Software designer can get the benefit of hardware without needing full knowledge
  - Hardware designer can quickly prototype hardware components
- Benchmarks for these complicated system need to be created
  - Standard algorithms common in embedded design like Coremax for processors
  - Have to take into account the complex nature of system. Limitless ways to implement different algorithms...
References


Questions?