Reduction of Control Hazards (Branch) Stalls with Dynamic Branch Prediction

- So far we have dealt with control hazards in instruction pipelines by:
  - Assuming that the branch is not taken (i.e stall when branch is taken).
  - Reducing the branch penalty by resolving the branch early in the pipeline
    - Branch penalty if branch is taken = stage resolved - 1
  - Branch delay slot and canceling branch delay slot. (ISA support needed)
  - Compiler-based static branch prediction encoded in branch instructions
    - Prediction is based on program profile or branch direction
    - ISA support needed.

How to further reduce the impact of branches on pipeline processor performance?

- **Dynamic Branch Prediction:**
  - Hardware-based schemes that utilize run-time behavior of branches to make dynamic predictions:
    - Information about outcomes of previous occurrences of branches are used to dynamically predict the outcome of the current branch.

- **Branch Target Buffer (BTB):** *(Goal: zero stall taken branches)*
  - A hardware mechanism that aims at reducing the stall cycles resulting from correctly predicted taken branches to zero cycles.
Static Conditional Branch Prediction

- Branch prediction schemes can be classified into static (at compilation time) and dynamic (at runtime) schemes.
- Static methods are carried out by the compiler. They are static because the prediction is already known before the program is executed.
- Static Branch prediction is encoded in branch instructions using one prediction (or branch direction hint) bit = 0 = Not Taken, = 1 = Taken
  - Must be supported by ISA, Ex: HP PA-RISC, PowerPC, UltraSPARC

Two basic methods to statically predict branches at compile time:

1 - Use the direction of a branch to base the prediction on. Predict backward branches (branches which decrease the PC) to be taken (e.g. loops) and forward branches (branches which increase the PC) not to be taken.

2 - Profiling can also be used to predict the outcome of a branch.

  - A number runs of the program are used to collect program behavior information (i.e. if a given branch is likely to be taken or not)
  - This information is included in the opcode of the branch (one bit branch direction hint) as the static prediction.

Static prediction was previously discussed in lecture 2
4th edition: in Chapter 2.3, 3rd Edition: In Chapter 4.2
More Loops in FP Code

(Misprediction rates for SPEC92)

Integer
Average 15% (i.e. 85% Prediction Accuracy)

Floating Point
Average 9% (i.e. 91% Prediction Accuracy)

F P has more loops

Misprediction rate for a profile-based predictor varies widely but is generally better for the FP programs, which have an average misprediction rate of 9% with a standard deviation of 4%, than for the integer programs, which have an average misprediction rate of 15% with a standard deviation of 5%.
Dynamic Conditional Branch Prediction

**Dynamic Conditional Branch Prediction**

- Dynamic branch prediction schemes are different from static mechanisms because they utilize hardware-based mechanisms that use the run-time behavior of branches to make more accurate predictions than possible using static prediction.

- Usually information about outcomes of previous occurrences of branches (branching history) is used to dynamically predict the outcome of the current branch. The two main types of dynamic branch prediction are:

  1. **One-level or Bimodal:** Usually implemented as a Pattern History Table (PHT), a table of usually two-bit saturating counters which is indexed by a portion of the branch address (low bits of address). (First proposed mid 1980s)
     - Also called *non-correlating* dynamic branch predictors.

  2. **Two-Level Adaptive Branch Prediction.** (First proposed early 1990s).
     - Also called *correlating* dynamic branch predictors.

- To reduce the stall cycles resulting from correctly predicted taken branches to zero cycles, a Branch Target Buffer (BTB) that includes the addresses of conditional branches that were taken along with their targets is added to the fetch stage.

---

**How?**

**Why?**

No ISA Support Needed

BTB discussed next

4th Edition: Dynamic Prediction in Chapter 2.3, BTB in Chapter 2.9
(3rd Dynamic Prediction in Chapter 3.4, BTB in Chapter 3.5)
Branch Target Buffer (BTB)

- Effective branch prediction requires the target of the branch at an early pipeline stage. (resolve the branch early in the pipeline)
  - One can use additional adders to calculate the target, as soon as the branch instruction is decoded. This would mean that one has to wait until the ID stage before the target of the branch can be fetched, taken branches would be fetched with a one-cycle penalty (this was done in the enhanced MIPS pipeline Fig A.24).

- To avoid this problem and to achieve zero stall cycles for taken branches, one can use a Branch Target Buffer (BTB).

- A typical BTB is an associative memory where the addresses of taken branch instructions are stored together with their target addresses.

- The BTB is accessed in Instruction Fetch (IF) cycle and provides answers to the following questions while the current instruction is being fetched:
  1. Is the instruction a branch?
  2. If yes, is the branch predicted taken?
  3. If yes, what is the branch target?

- Instructions are fetched from the target stored in the BTB in case the branch is predicted-taken and found in BTB.

- After the branch has been resolved the BTB is updated. If a branch is encountered for the first time a new entry is created once it is resolved as taken.

Goal of BTB: Zero stall taken branches
Basic Branch Target Buffer (BTB)

- **Branch Address**
- **Branch Target**
  - if predicted taken

- **Look Up**
- **PC of instruction to fetch**
- **Fetch instruction from instruction memory (I-L1 Cache)**
- **Predicted PC**
  - 0 = NT = Not Taken
  - 1 = T = Taken

- **Branch Targets**
  - Branch predicted taken or untaken

- **Number of entries in branch-target buffer**

- **Instruction Fetch**
- **BTB is accessed in Instruction Fetch (IF) cycle**

- **Goal of BTB**: Zero stall taken branches

- **Is the instruction a branch?**

- **Branch Taken?**

- **No**: instruction is not predicted to be branch. Proceed normally
  - i.e. target

- **Yes**: then instruction is branch and predicted PC should be used as the next PC
  - i.e. target
Here, branches are assumed to be resolved in ID

**BTB Operation**

- **IF**
  - Send PO to memory and branch-target buffer
  - Instruction Memory (cache)

- **BTB Lookup**
  - Entry found in branch-target buffer?
    - No
    - Yes

- **ID**
  - Is instruction a taken branch?
    - No
      - Normal instruction execution
    - Yes
      - Send out predicted PC

- **EX**
  - Taken branch?
    - No
    - Yes
      - Brand correctly predicted; continue execution with no stalls

**Update BTB**

- Misspredicted branch, kill fetched instruction; restart fetch at other target; delete entry from target buffer
- Brand correctly predicted; continue execution with no stalls

One more stall to update BTB
Penalty = 1 + 1 = 2 cycles
# Branch Penalty Cycles Using A Branch-Target Buffer (BTB)

Base Pipeline Taken Branch Penalty = 1 cycle (*i.e. branches resolved in ID*)

<table>
<thead>
<tr>
<th>Instruction in buffer</th>
<th>Prediction</th>
<th>Actual branch</th>
<th>Penalty cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes</td>
<td>Taken</td>
<td>Taken</td>
<td>0</td>
</tr>
<tr>
<td>Yes</td>
<td>Taken</td>
<td>Not taken</td>
<td>2</td>
</tr>
<tr>
<td>No</td>
<td>Taken</td>
<td></td>
<td>2</td>
</tr>
</tbody>
</table>

*BTB Goal: Taken Branches with zero stalls*

Assuming one more stall cycle to update BTB
Penalty = 1 + 1 = 2 cycles

Penalties for all possible combinations of whether the branch is in the buffer and what it actually does, assuming we store only taken branches in the buffer.
Basic Dynamic Branch Prediction

- Simplest method: (One-Level or Non-Correlating)
  - A branch prediction buffer or Pattern History Table (PHT) indexed by low address bits of the branch instruction.
  - Each buffer location (or PHT entry or predictor) contains one bit indicating whether the branch was recently taken or not.
    - e.g. 0 = not taken, 1 = taken
  - Always mispredicts in first and last loop iterations.

- To improve prediction accuracy, two-bit prediction is used:
  - A prediction must miss twice before it is changed.
    - Thus, a branch involved in a loop will be mispredicted only once when encountered the next time as opposed to twice when one bit is used.
  - Two-bit prediction is a specific case of n-bit saturating counter incremented when the branch is taken and decremented when the branch is not taken.
    - Two-bit saturating counters (predictors) are usually always used based on observations that the performance of two-bit PHT prediction is comparable to that of n-bit predictors.
One-Level Bimodal Branch Predictors
Pattern History Table (PHT)

Table (PHT) has $2^N$ entries
(also called predictors).

Indexed by
$N$ Low Bits of Branch Address

Number of bits needed = $2 \times 4k = 8k$ bits

High bit determines branch prediction
0 = NT = Not Taken
1 = T = Taken

What if different branches map to the same predictor (counter)?
This is called branch address aliasing and leads to interference with current branch prediction by other branches and may lower branch prediction accuracy for programs with aliasing.
Basic Dynamic Two-Bit Branch Prediction:

Two-bit Predictor State Transition Diagram (in textbook):

- **0 0**: Not Taken (NT)
- **0 1**: Not Taken (NT)
- **1 0**: Taken (T)
- **1 1**: Taken (T)

Or Two-bit saturating counter predictor state transition diagram (Smith Algorithm):

- **00**: Not Taken (NT)
- **01**: Not Taken (NT)
- **10**: Not Taken (NT)
- **11**: Taken (T)

The two-bit predictor used is updated after the branch is resolved.
Prediction Accuracy of A 4096-Entry Basic One-Level Dynamic Two-Bit Branch Predictor

Has, more branches involved in IF-Then-Else constructs the FP

N=12
$2^N = 4096$

**SPEC89 benchmarks**

<table>
<thead>
<tr>
<th>FP</th>
<th>Frequency</th>
<th>Misprediction Rate:</th>
</tr>
</thead>
<tbody>
<tr>
<td>nasa7</td>
<td>1%</td>
<td>(Lower misprediction rate due to more loops)</td>
</tr>
<tr>
<td>matrix300</td>
<td>0%</td>
<td></td>
</tr>
<tr>
<td>tomcatv</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>doduc</td>
<td>5%</td>
<td></td>
</tr>
<tr>
<td>spice</td>
<td>9%</td>
<td></td>
</tr>
<tr>
<td>fpppp</td>
<td>9%</td>
<td></td>
</tr>
<tr>
<td>gcc</td>
<td>12%</td>
<td></td>
</tr>
<tr>
<td>espresso</td>
<td>5%</td>
<td></td>
</tr>
<tr>
<td>eqntott</td>
<td>18%</td>
<td></td>
</tr>
<tr>
<td>li</td>
<td>10%</td>
<td></td>
</tr>
</tbody>
</table>

**Integer**

**FP**

Integer average 11%
FP average 4%

Prediction accuracy of a 4096-entry two-bit prediction buffer for the SPEC89 benchmarks.
From The Analysis of Static Branch Prediction:
MIPS Performance Using Canceling Delay Branches

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>% conditional branches</th>
<th>% conditional branches with empty slots</th>
<th>% conditional branches that are cancelling</th>
<th>% cancelling branches that are cancelled</th>
<th>% branches with cancelled delay slots</th>
<th>Total % branches with empty or cancelled delay slot</th>
</tr>
</thead>
<tbody>
<tr>
<td>compress</td>
<td>14%</td>
<td>18%</td>
<td>31%</td>
<td>43%</td>
<td>13%</td>
<td>31%</td>
</tr>
<tr>
<td>eqntott</td>
<td>24%</td>
<td>24%</td>
<td>50%</td>
<td>24%</td>
<td>12%</td>
<td>36%</td>
</tr>
<tr>
<td>espresso</td>
<td>15%</td>
<td>29%</td>
<td>19%</td>
<td>21%</td>
<td>4%</td>
<td>33%</td>
</tr>
<tr>
<td>gcc</td>
<td>15%</td>
<td>16%</td>
<td>33%</td>
<td>34%</td>
<td>11%</td>
<td>27%</td>
</tr>
<tr>
<td>li</td>
<td>15%</td>
<td>20%</td>
<td>55%</td>
<td>48%</td>
<td>26%</td>
<td>46%</td>
</tr>
<tr>
<td>Integer average</td>
<td>17%</td>
<td>21%</td>
<td>38%</td>
<td>34%</td>
<td>13%</td>
<td>35%</td>
</tr>
<tr>
<td>d馗duc</td>
<td>8%</td>
<td>33%</td>
<td>12%</td>
<td>62%</td>
<td>8%</td>
<td>41%</td>
</tr>
<tr>
<td>ear</td>
<td>10%</td>
<td>37%</td>
<td>36%</td>
<td>14%</td>
<td>5%</td>
<td>42%</td>
</tr>
<tr>
<td>hydro2d</td>
<td>12%</td>
<td>0%</td>
<td>69%</td>
<td>24%</td>
<td>16%</td>
<td>17%</td>
</tr>
<tr>
<td>mdljdp2</td>
<td>9%</td>
<td>0%</td>
<td>86%</td>
<td>10%</td>
<td>8%</td>
<td>8%</td>
</tr>
<tr>
<td>su2cor</td>
<td>3%</td>
<td>7%</td>
<td>17%</td>
<td>57%</td>
<td>10%</td>
<td>17%</td>
</tr>
<tr>
<td>FP average</td>
<td>8%</td>
<td>16%</td>
<td>44%</td>
<td>34%</td>
<td>9%</td>
<td>25%</td>
</tr>
<tr>
<td>Overall average</td>
<td>12%</td>
<td>18%</td>
<td>41%</td>
<td>34%</td>
<td>11%</td>
<td>30%</td>
</tr>
</tbody>
</table>

Delayed and cancelling delay branches for MIPS allow branch hazards to be hidden 70% of the time on average for these 10 SPEC benchmarks.

70% Static Branch Prediction Accuracy

(repeated here from lecture2)
Prediction Accuracy of Basic One-Level Two-Bit Branch Predictors:

4096-entry buffer (PHT) Vs. An Infinite Buffer Under SPEC89

Conclusion: SPEC89 programs do not have many branches that suffer from branch address aliasing (interference) when using a 4096-entry PHT. Thus increasing PHT size (which usually lowers aliasing) did not result in major prediction accuracy improvement.
Correlating Branches

Recent branches are possibly correlated: The behavior of recently executed branches affects prediction of current branch.

Example:

B1 if (aa==2)
   aa=0; (not taken)
       B1        DSUBUI R3, R1, #2 ; R3 = R1 - 2
       BNEZ     R3, L1  ; B1 (aa!=2)

B2 if (bb==2)
   bb=0; (not taken)
       B2        DSUBUI R3, R2, #2 ; R3 = R2 - 2
       BNEZ     R3, L2  ; B2 (bb!=2)
       DADD     R2, R0, R0 ; bb==0

B3 if (aa!==bb){
   (not taken)
   B3        DSUBUI R3, R1, R2 ; R3=aa-bb

Branch B3 is correlated with branches B1, B2. If B1, B2 are both not taken, then B3 will be taken. Using only the behavior of one branch cannot detect this behavior.

Both B1 and B2 Not Taken → B3 Taken
Correlating Two-Level Dynamic GAp Branch Predictors

- Improve branch prediction by looking not only at the history of the branch in question but also at that of other branches using two levels of branch history.
- Uses two levels of branch history:

1. **First level (global):**
   - Record the global pattern or history of the m most recently executed branches as taken or not taken. Usually an m-bit shift register.

2. **Second level (per branch address):**
   - \(2^m\) prediction tables, each table entry has n-bit saturating counter.
   - The branch history pattern from first level is used to select the proper branch prediction table in the second level.
   - The low N bits of the branch address are used to select the correct prediction entry (predictor) within a the selected table, thus each of the \(2^m\) tables has \(2^N\) entries and each entry is 2 bits counter.
   - Total number of bits needed for second level = \(2^m \times n \times 2^N\) bits

- In general, the notation: \(\text{GAp (m,n)}\) predictor means:
  - Record last m branches to select between \(2^m\) history tables.
  - Each second level table uses n-bit counters (each table entry has n bits).
- Basic two-bit single-level Bimodal BHT is then a (0,2) predictor.
Organization of A Correlating Two-level GAp (2,2) Branch Predictor

First Level
Branch History Register (BHR)
(2 bit shift register)

2-bit global branch history

(N=4)
Low 4 bits of address

(n = 2)
2-bit per branch predictors

Selects correct table

Second Level
Pattern History Tables (PHTs)

m = # of branches tracked in first level = 2
Thus \(2^m = 2^2 = 4\) tables in second level

N = # of low bits of branch address used = 4
Thus each table in 2nd level has \(2N = 24 = 16\) entries

n = # number of bits of 2nd level table entry = 2
Number of bits for 2nd level = \(2^m \times n \times 2^N\)
= \(4 \times 2 \times 16 = 128\) bits

Patterns: 00, 01, 10, 11

High bit determines branch prediction
0 = Not Taken
1 = Taken

Low 4 bits of address selects correct table

A (2,2) branch-prediction buffer uses a two-bit global history to choose from among four predictors for each branch address.

GAp (m,n) here m=2 n=2 Thus Gap (2,2)
Dynamic Branch Prediction: Example

if (d==0)
    d=1;
if (d==1)
    \ldots

L1:
    DADDIU R1, R0, #1
    BNEZ R1, L1 ; branch b1 (d!=0)

L2:
    DADDIU R3, R1, # -1
    BNEZ R3, L2 ; branch b2 (d!=1)

Possible execution sequences for a code fragment.

<table>
<thead>
<tr>
<th>Initial value of d</th>
<th>d==0?</th>
<th>b1</th>
<th>Value of d before b2</th>
<th>d==1?</th>
<th>b2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Yes</td>
<td>Not taken</td>
<td>1</td>
<td>Yes</td>
<td>Not taken</td>
</tr>
<tr>
<td>1</td>
<td>No</td>
<td>Taken</td>
<td>1</td>
<td>Yes</td>
<td>Not taken</td>
</tr>
<tr>
<td>2</td>
<td>No</td>
<td>Taken</td>
<td>2</td>
<td>No</td>
<td>Taken</td>
</tr>
</tbody>
</table>

Behavior of a one-bit predictor initialized to not taken.

<table>
<thead>
<tr>
<th>d=?</th>
<th>b1 prediction</th>
<th>b1 action</th>
<th>New b1 prediction</th>
<th>b2 prediction</th>
<th>b2 action</th>
<th>New b2 prediction</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NT</td>
<td>T</td>
<td>T</td>
<td>NT</td>
<td>T</td>
<td>T</td>
</tr>
<tr>
<td>0</td>
<td>T</td>
<td>NT</td>
<td>NT</td>
<td>T</td>
<td>NT</td>
<td>NT</td>
</tr>
<tr>
<td>2</td>
<td>NT</td>
<td>T</td>
<td>T</td>
<td>NT</td>
<td>T</td>
<td>T</td>
</tr>
<tr>
<td>0</td>
<td>T</td>
<td>NT</td>
<td>NT</td>
<td>T</td>
<td>NT</td>
<td>NT</td>
</tr>
</tbody>
</table>

One Level with one-bit table entries (predictors):

NT = 0 = Not Taken
T = 1 = Taken
Dynamic Branch Prediction: Example (continued)

if (d==0)
  d=1;
if (d==1)

BNEZ R1, L1 ; branch b1 (d!=0)
DADDIU R1, R0, #1 ; d==0, so d=1
L1:
DADDIU R3, R1, # -1
BNEZ R3, L2 ; branch b2 (d!=1)

. . .

L2:

Combinations and meaning of the taken/not taken prediction bits.

<table>
<thead>
<tr>
<th>Initial value of d</th>
<th>d==0?</th>
<th>b1</th>
<th>Value of d before b2</th>
<th>d==1?</th>
<th>b2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Yes</td>
<td>Not taken</td>
<td>1</td>
<td>Yes</td>
<td>Not taken</td>
</tr>
<tr>
<td>1</td>
<td>No</td>
<td>Taken</td>
<td>1</td>
<td>Yes</td>
<td>Not taken</td>
</tr>
<tr>
<td>2</td>
<td>No</td>
<td>Taken</td>
<td>2</td>
<td>No</td>
<td>Taken</td>
</tr>
</tbody>
</table>

The action of the one-bit predictor with one bit of correlation, initialized to not taken/not taken.

<table>
<thead>
<tr>
<th>d=?</th>
<th>b1 prediction</th>
<th>b1 action</th>
<th>New b1 prediction</th>
<th>b2 prediction</th>
<th>b2 action</th>
<th>New b2 prediction</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NT/NT</td>
<td>T</td>
<td>T/NT</td>
<td>NT/NT</td>
<td>T</td>
<td>NT/NT</td>
</tr>
<tr>
<td>0</td>
<td>T/NT</td>
<td>NT</td>
<td>T/NT</td>
<td>NT/NT</td>
<td>NT</td>
<td>NT/NT</td>
</tr>
<tr>
<td>2</td>
<td>T/NT</td>
<td>T</td>
<td>T/NT</td>
<td>NT/NT</td>
<td>T</td>
<td>NT/NT</td>
</tr>
<tr>
<td>0</td>
<td>T/NT</td>
<td>NT</td>
<td>T/NT</td>
<td>NT/NT</td>
<td>NT</td>
<td>NT/NT</td>
</tr>
</tbody>
</table>

Two level Gap(1,1)

m = 1
n = 1
Prediction Accuracy of Two-Bit Dynamic Predictors Under SPEC89
MCFarling's gshare Predictor

gshare = global history with index sharing

- McFarling noted (1993) that using global history information might be less efficient than simply using the address of the branch instruction, especially for small predictors.
- He suggests using both global history (BHR) and branch address by hashing them together. He proposed using the XOR of global branch history register (BHR) and branch address since he expects that this value has more information than either one of its components. The result is that this mechanism outperforms GAp scheme by a small margin.
- This mechanism uses less hardware than GAp, since both branch history (first level) and pattern history (second level) are kept globally.
- The hardware cost for k history bits is $k + 2 \times 2^k$ bits, neglecting costs for logic.

gshare is one of the most widely implemented two level dynamic branch prediction schemes
gshare Predictor

Branch and pattern history are kept globally. History and branch address are XORed and the result is used to index the pattern history table.

First Level:

(BHR)
Branch History Shift Register

Second Level:

XOR (bitwise XOR)

2-bit saturating counters (predictors)

Index the second level

One Pattern History Table (PHT) with $2^k$ entries (predictors)

Here:

$m = N = k$

gshare = global history with index sharing
Hybrid Predictors

(Also known as tournament or combined predictors)

- Hybrid predictors are simply combinations of two (most common) or more branch prediction mechanisms.
- This approach takes into account that different mechanisms may perform best for different branch scenarios.
- McFarling presented (1993) a number of different combinations of two branch prediction mechanisms.
- He proposed to use an additional 2-bit counter selector array which serves to select the appropriate predictor for each branch.
- One predictor is chosen for the higher two counts, the second one for the lower two counts. The selector array counter used is updated as follows:
  1. If the first predictor is wrong and the second one is right the selector counter used counter is decremented,
  2. If the first one is right and the second one is wrong, the selector counter used is incremented.
  3. No changes are carried out to selector counter used if both predictors are correct or wrong.
A Generic Hybrid Predictor

Usually only two predictors are used (i.e. n = 2) e.g. As in Alpha, IBM POWER 4-7
MCFarling’s Hybrid Predictor Structure

The hybrid predictor contains an additional counter array (selector array) with 2-bit up/down saturating counters. Which serves to select the best predictor to use. Each counter in the selector array keeps track of which predictor is more accurate for the branches that share that counter. Specifically, using the notation P1c and P2c to denote whether predictors P1 and P2 are correct respectively, the selector counter is incremented or decremented by P1c-P2c as shown.

<table>
<thead>
<tr>
<th></th>
<th>P1c</th>
<th>P2c</th>
<th>P1c-P2c</th>
</tr>
</thead>
<tbody>
<tr>
<td>Both wrong</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P2 correct</td>
<td>0</td>
<td>1</td>
<td>-1</td>
</tr>
<tr>
<td>P1 correct</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Both correct</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(no change)  (decrement counter)  (increment counter)  (no change)

Branch Address
(N Low Bits)

PC

Here two predictors are combined

Selector Array

P1c-P2c

Select Counter Update

11
10
Use P1

Counts

01
00
Use P2

useP1

P1

e.g gshare

e.g One level

P2

(Current example implementations: IBM POWER4, 5, 6)
MCFarling’s Hybrid Predictor Performance by Benchmark

Conditional Branch Prediction Accuracy (%)

- doduc
- eqntott
- espress
- fpppp
- gcc
- li
- mat300
- nasa7
- spice
- tomatcv
- average

bimodal (Single Level)
gshare
bimodal/gshare (Combined)
# Processor Branch Prediction Examples

<table>
<thead>
<tr>
<th>Processor</th>
<th>Released</th>
<th>Accuracy</th>
<th>Prediction Mechanism</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyrix 6x86</td>
<td>early '96</td>
<td>ca. 85%</td>
<td>PHT associated with BTB</td>
</tr>
<tr>
<td>Cyrix 6x86MX</td>
<td>May '97</td>
<td>ca. 90%</td>
<td>PHT associated with BTB</td>
</tr>
<tr>
<td>AMD K5</td>
<td>mid '94</td>
<td>80%</td>
<td>PHT associated with I-cache</td>
</tr>
<tr>
<td>AMD K6</td>
<td>early '97</td>
<td>95%</td>
<td>2-level adaptive associated with BTIC and ALU</td>
</tr>
<tr>
<td>Intel Pentium</td>
<td>late '93</td>
<td>78%</td>
<td>PHT associated with BTB</td>
</tr>
<tr>
<td>Intel P6</td>
<td>mid '96</td>
<td>90%</td>
<td>2 level adaptive with BTB</td>
</tr>
<tr>
<td>PowerPC750</td>
<td>mid '97</td>
<td>90%</td>
<td>PHT associated with BTIC</td>
</tr>
<tr>
<td>MC68060</td>
<td>mid '94</td>
<td>90%</td>
<td>PHT associated with BTIC</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>early '97</td>
<td>95%</td>
<td>Hybrid 2-level adaptive associated with I-cache</td>
</tr>
<tr>
<td>HP PA8000</td>
<td>early '96</td>
<td>80%</td>
<td>PHT associated with BTB</td>
</tr>
<tr>
<td>SUN UltraSparc</td>
<td>mid '95</td>
<td>88%int 94%FP</td>
<td>PHT associated with I-cache</td>
</tr>
</tbody>
</table>

PHT = One Level

S+D : Uses both static (ISA supported) and dynamic branch prediction