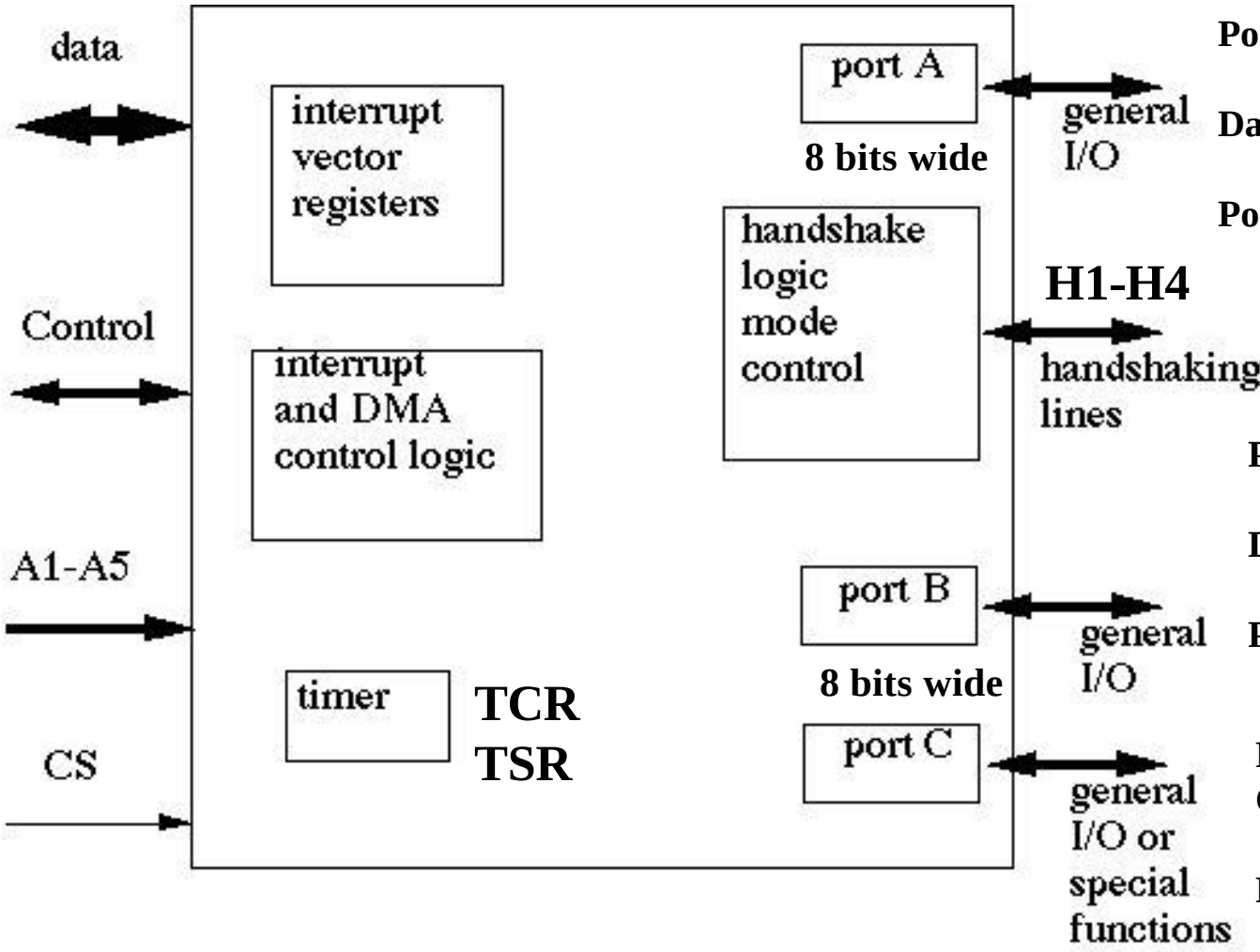
The Motorola 68230 Parallel Interface Timer (PI/T)

- **A general purpose Parallel Interface and Timer, PI/T chip that offer several *very complex* modes of operation.**



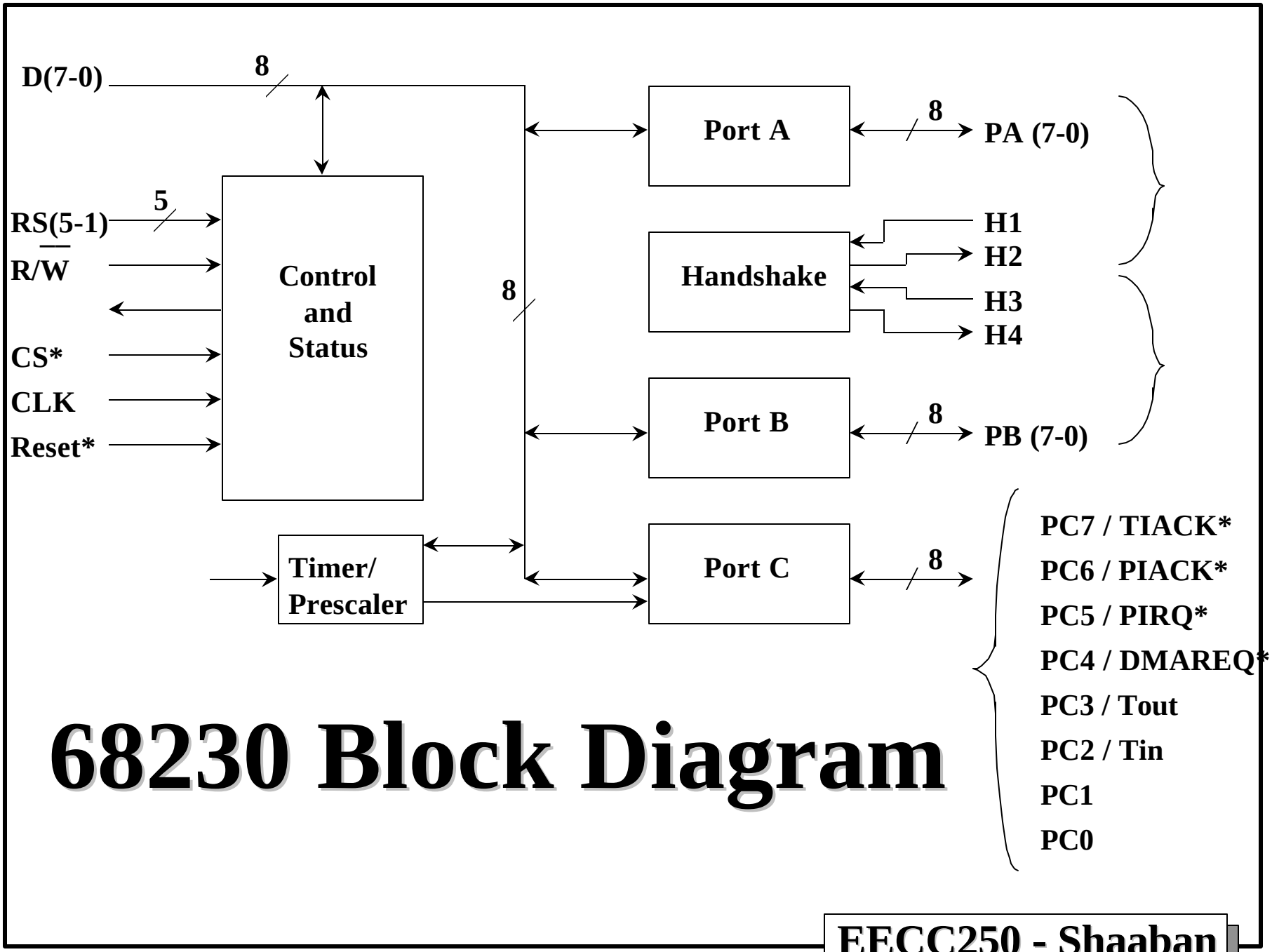
Port A

Port A Data Register,
PADR: $0FF010
Data Direction Register,
PADDR: $0FF004
Port A Control Register,
PACR: $0FF00C

Port B

Port B Data Register,
PBDR: $0FF012
Data Direction Register:
PBDDR: $0FF006
Port B Control Register,
PBCR: $0FF00E

Port General Control Register
PGCR: $0FF000
Port Status Register
PSR: $0FF1A

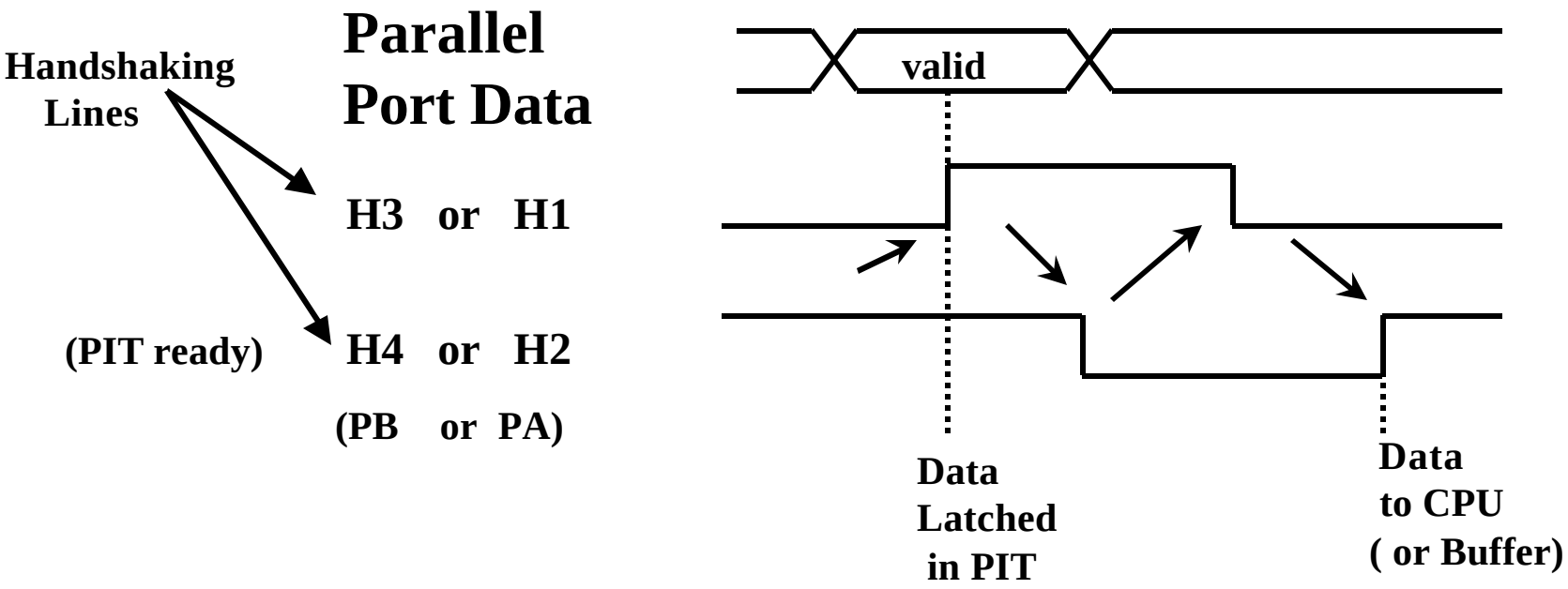


68230 Block Diagram

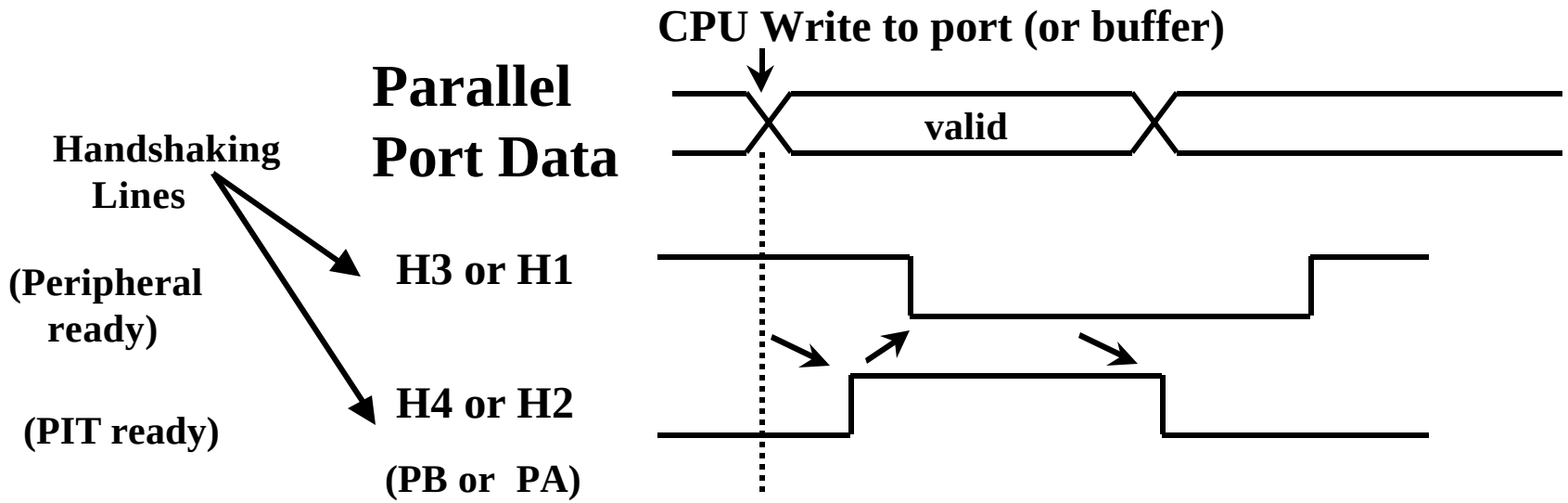
68230 Registers Address Equates

```
PIT     EQU   $0FF000     Base Address of PI/T
PGCR    EQU   PIT         Address of Port General Control Register
PSRR    EQU   PIT+2       Port service request register
PADDR   EQU   PIT+4       Data direction register A
PBDDR   EQU   PIT+6       Data direction register B
PACR    EQU   PIT+$0C     Port A control register
PBCR    EQU   PIT+$0E     Port B control register
PADR    EQU   PIT+$10     Port A data register
PBDR    EQU   PIT+$12     Port B data register
PSR     EQU   PIT+$1A     Port status register
TCR     EQU   PIT+$20     Timer control register
TSR     EQU   PIT+$34     Timer status register
```

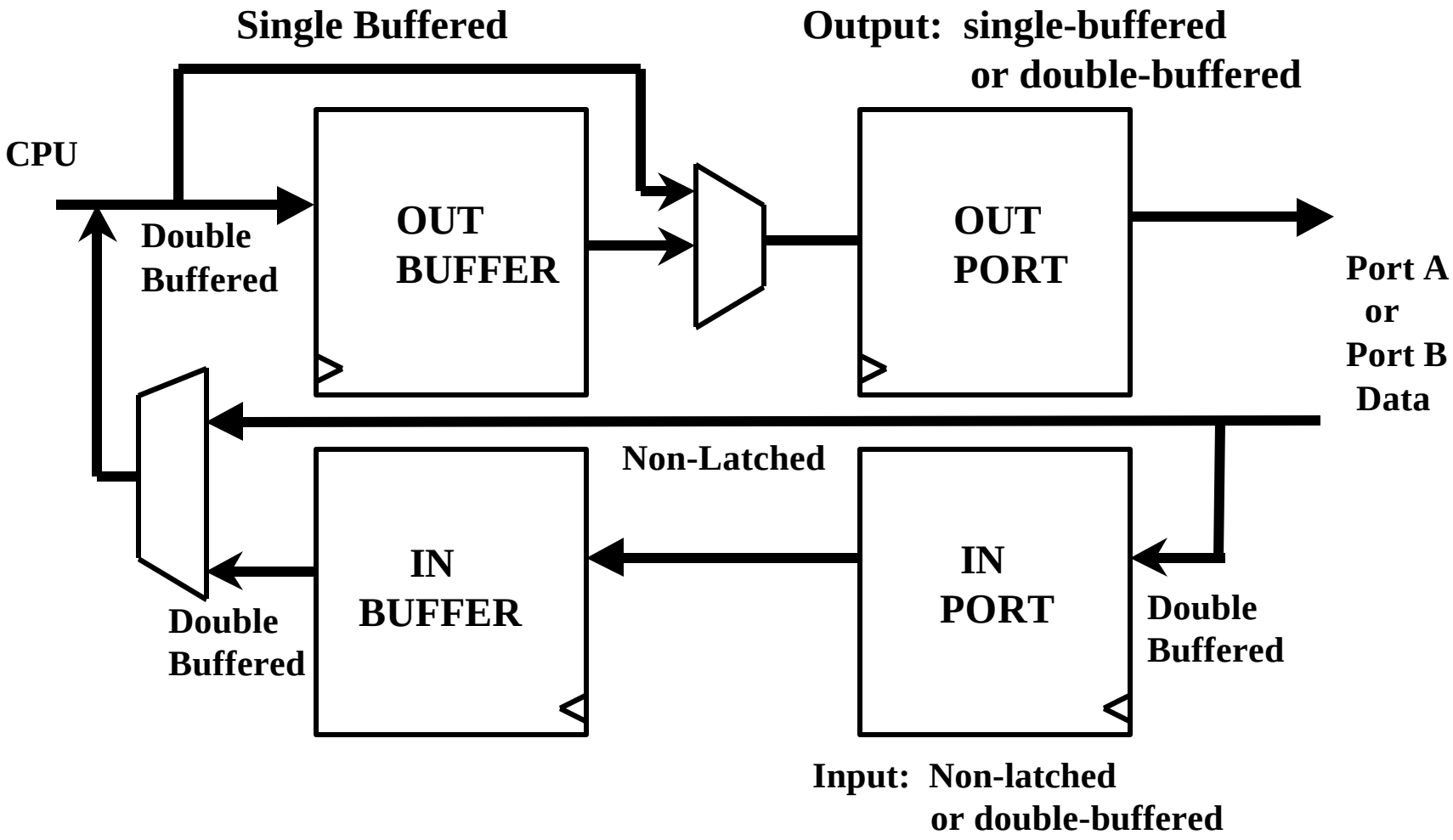
68230 Parallel I/O
Input Handshake Timing



68230 Parallel I/O Output Handshake Timing



68230 Parallel I/O Data Latching/Buffering



68230 PIT Parallel I/O Modes

- **Mode 0**
  - **Unidirectional 8-bit, separate PA & PB**
    - **Submode 00 - Double Buffered in, Single Buffered out**
    - **Submode 01 - Non-Latched in, Double Buffered out**
    - **Submode 1X - Non-Latched in, Single Buffered out**
- **Mode 1**
  - **Unidirectional 16-bit, combined PA**
    - **Submode X0 - Double Buffered (DB) in, Single Buffered out**
    - **Submode X1 - Non-latched (NL) in, Double Buffered (DB) out**
- **Mode 2**
  - **Bidirectional 8-bit, separate PA & PB**
    - **Port A - NL in, SB out (No handshake, unidirectional per bit)**
    - **Port B - DB bidirectional (H1, H2 for output & H3, H4 for input)**
- **Mode 3**
  - **Bidirectional 16-bit, combined PA & PB**
    - **PA & PB - DB bidirectional (H1, H2 for output & H3, H4 for input)**

Format of Port General Control Register
PGCR

PGCR7 PGCR6	PGCR5 PGCR4	PGCR3 PGCR2 PGCR1 PGCR0
Port Mode Control	H34 H12	H4 H3 H2 H1
00 Mode 0	Enable Enable	sense sense sense sense
01 Mode 1		
10 Mode 2	0 Disable	0 Active low
11 Mode 3	1 Enable	1 Active high

Example:

PGCR = %00110000

Means:

Mode 0, Unidirectional 8-bit, separate PA & PB
Both H34 and H12 handshaking enabled
H4-H4 active low

PACR Format of Port A Control Register in Mode 0

PACR7 PACR6	PACR5 PACR4 PACR3	PACR2	PACR1 PACR0
Submode: 00 submode 0 01 submode 1 10 submode 1x	H2 Control 0xx Edge-sensitive input 100 output- negated 101 output - asserted 110 output - interlocked Handshake 111 Output - pulsed handshake	H2 Interrupt 0 Disabled 1 Enabled	H1 Control 0X H1 interrupt disabled 10 H1 interrupt enabled XX

Example: PACR = %00000000
PADDR = %00000000

Means: Port A is used as an input port
Submode 0 (Double Buffered input)
H2 Edge-sensitive
H2 interrupt disabled
H1 interrupt disabled

PBCR Format of Port B Control Register in Mode 0

PBCR7 PBCR6	PBCR5 PBCR4 PBCR3	PBCR2	PBCR1 PBCR0
Submode: 00 submode 0 01 submode 1 10 submode 1x	H4 Control 0xx Edge-sensitive input 100 output- negated 101 output - asserted 110 output - interlocked Handshake 111 Output - pulsed handshake	H4 Interrupt 0 Disabled 1 Enabled	H3 Control 0X H3 interrupt disabled 10 H3 interrupt enabled XX

Example: PBCR = %00000000
PBDDR = %11111111

Means: Port B is used as an output port
Submode 1 (Double Buffered output)
H4 Edge-sensitive
H4 interrupt disabled
H3 interrupt disabled

Port Status Register, PSR

- **Reflects activity of the handshake lines**

PSR

PSR7	PSR6	PSR5	PSR4	PSR3	PSR2	PSR1	PSR0
H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S

← Follow level of line → ← Set by line depending on mode →

PSR0-PSR3 must be cleared by the program by writing a 1 onto them

Example:

```
MOVE.B  #$0F,PSR
```

clears bits PSR0-PSR3

Example:

```
BTST.B #0,PSR
```

checks if status of H1

PI/T Handshaking Input Example

- **Continuously check the input handshaking line H1 of port A, if active a new data byte is read from port A and stored in a buffer in memory.**

```
        ORG       $1000
        MOVE.B    #$30,PGCR      Initialize PGCR to enable handshaking
        MOVE.B    #$80,PACR      Initialize port A, submode 1x
        MOVE.B    #$00, PADDR    Set Port A as input
        MOVE.B    #$0F,PSR       Clear PSR's four low status bits.
        LEA       BUFFER,A0      Load DATA address in A0
WAIT    MOVE.B    PSR,D0         Copy PSR into D0
        BTST.B    #0,D0          Check if bit 0 of PSR = 1
        BEQ       WAIT
        MOVE.B    PADR,D1        Get a byte from port A
        MOVE.B    D1,(A0)+       Store byte in memory buffer
        MOVE.B    #$0F,PSR       Clear PSR's four low status bits.
        BRA       WAIT           Busy-wait on H1 for more values
        STOP      #$2700
        ORG       $2000
BUFFER  DS.B      1000           Reserve 1000 bytes for buffer
        END       $1000
```