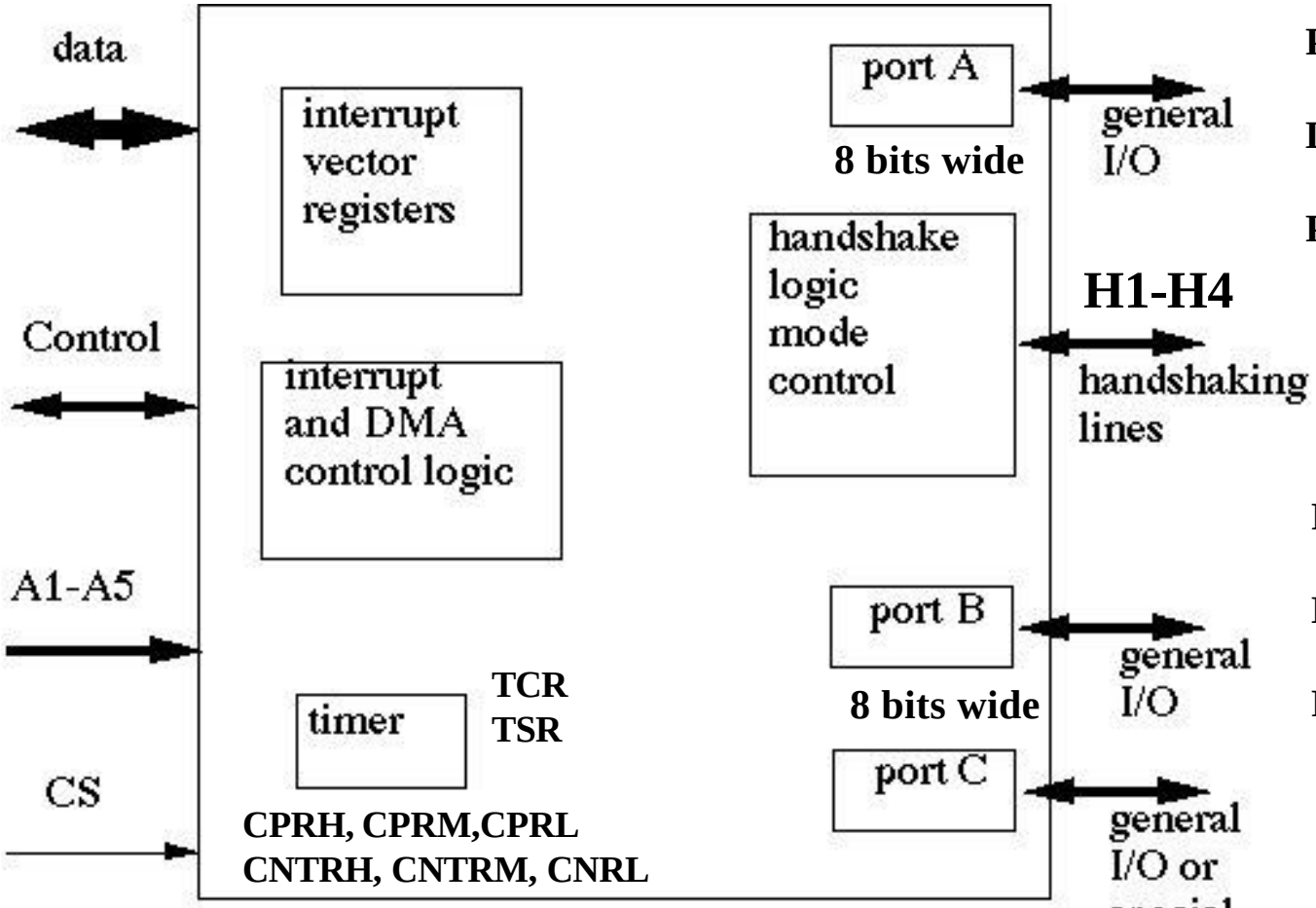
The Motorola 68230 PI/T



Timer Control Register (TCR): $0FF20
Timer Status Register (TSR) at : $0FF34
Counter preload register CPR: CPRH, CPRM, CPRL
Counter register CNTR: CNTRH, CNTRM, CNTRL

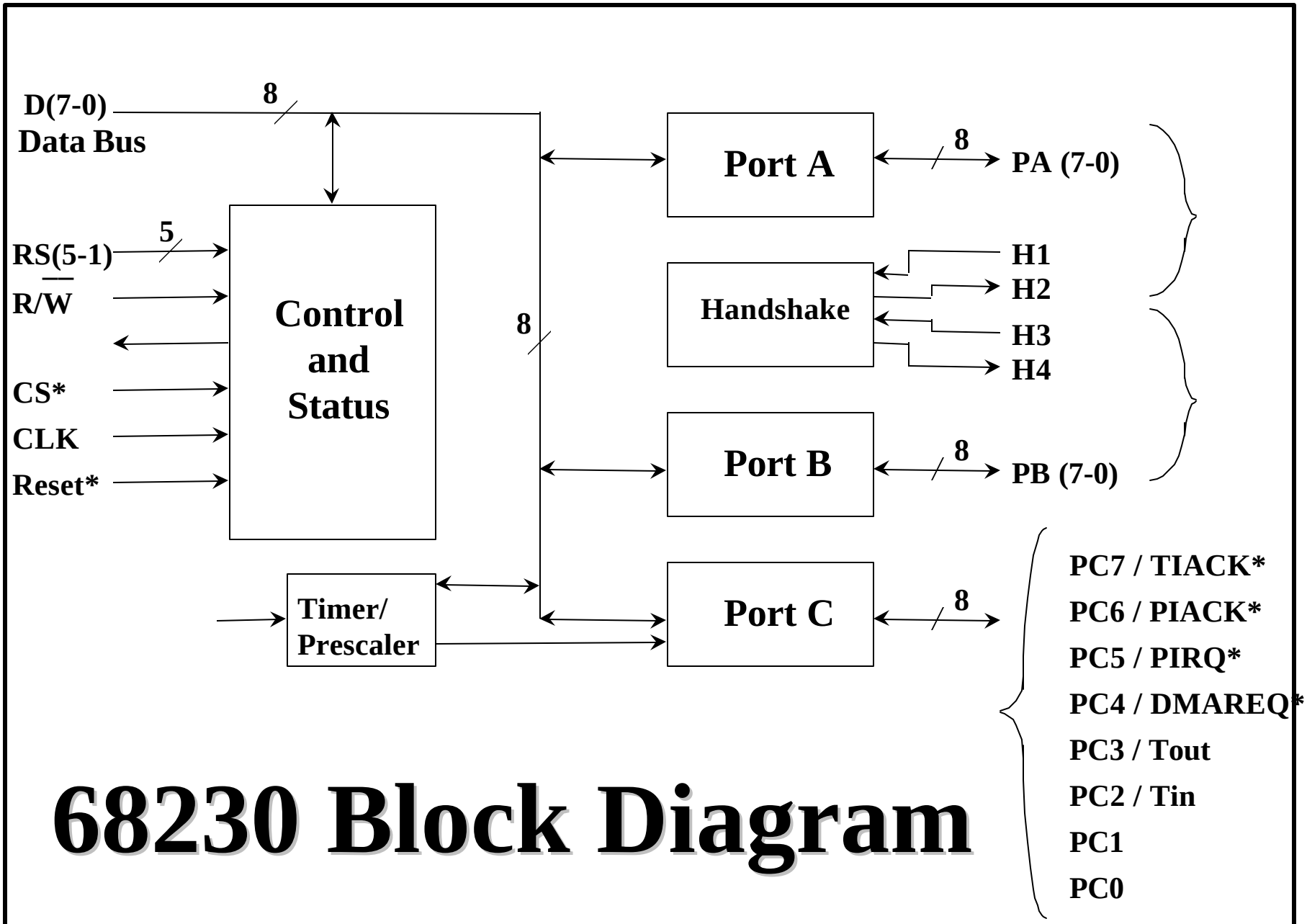
Port A

Port A Data Register,
PADR: $0FF010
Data Direction Register,
PADDR: $0FF004
Port A Control Register,
PACR: $0FF00C

Port B

Port B Data Register,
PBDR: $0FF012
Data Direction Register:
PBDDR: $0FF006
Port B Control Register,
PBCR: $0FF00E

Port General Control Register
PGCR: $0FF000
Port Status Register
PSR: $0FF1A

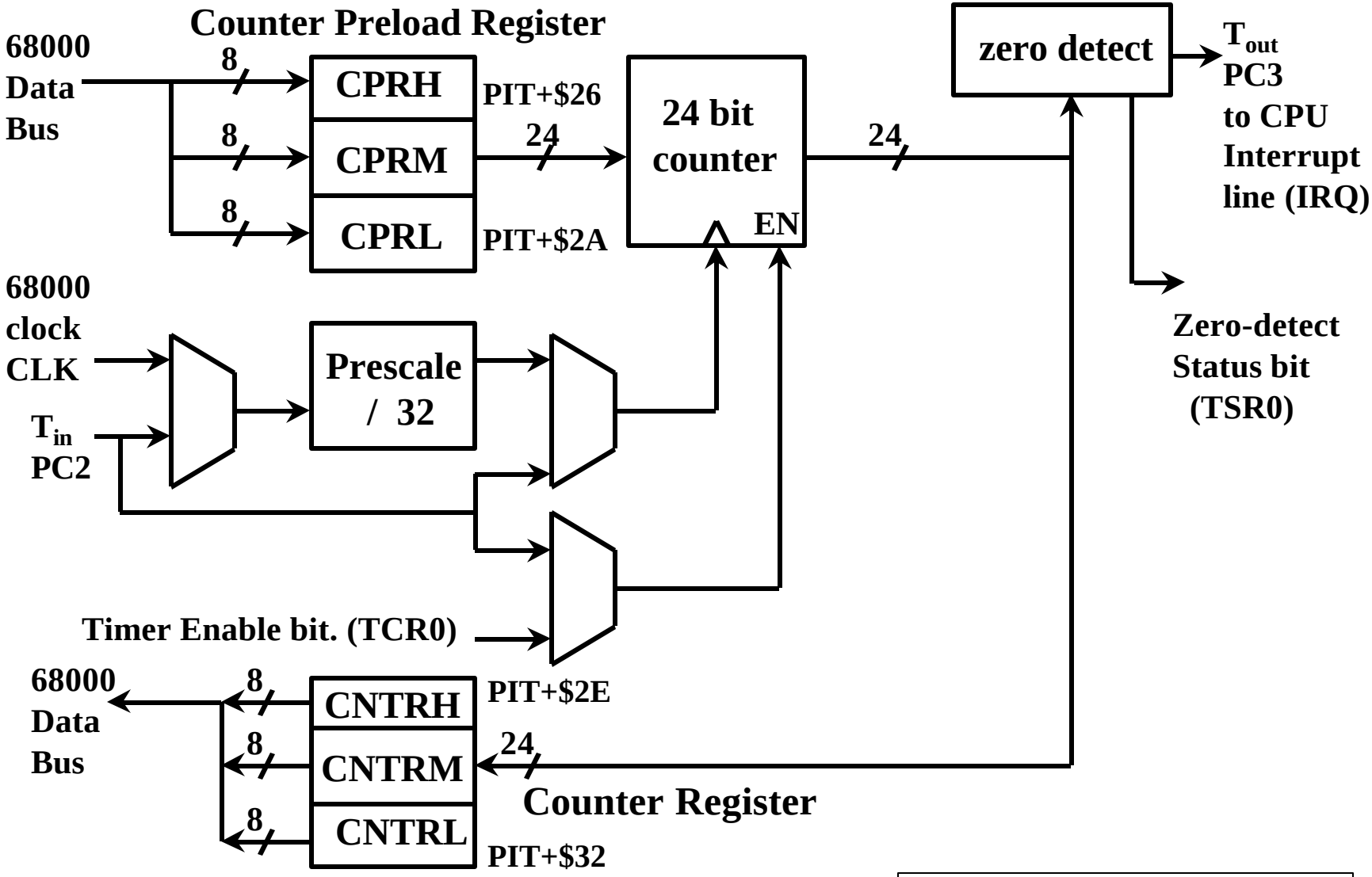


68230 Block Diagram

68230 PIT Timer Functions

- **Timers are devices which include a clocked counter which is usually decremented every clock cycle towards zero.**
- **By loading the counter with an initial value, one can generate a specific delay between staring the counter and the time it reaches zero.**
- **The 68230 uses a 24-bit counter for its timer functions.**
- **Functions Possible:**
  - **Generate square wave of any frequency (reload after reaching zero).**
  - **Generate single pulse of any width**
  - **Generate periodic interrupts to the CPU**
  - **Measure elapsed time (or frequency)**

68230 PIT Timer Block Diagram



68230 PIT Timer

- **Can be driven by 68000 clock as is, or divided by 32 (prescaled), or by an external clock connected to pin T_{in} (pin PC2 of port C).**
- **8-bit Timer Control Register (TCR) at: PIT + $20**
- **8-bit Timer Status Register (TSR) at : PIT + $34**
  - **When the counter reaches zero it sets the zero-detect Status, ZDS, (bit 0 of the TSR).**
  - **ZDS is set automatically and has to be cleared by writing a one into it.**
- **T_{out} (pin PC3 of port C) is usually connected to one of the 68000 interrupt lines and used to interrupt the CPU when count reaches zero.**
- **Counter preload register CPR: 3, 8-bit registers CPRH, CPRM, CPRL**
  - **Found at addresses: (PIT +$26, $28, $2A)**
  - **Address PIT + $24 has no real register but used as fake address for CPR to complete a long word.**
- **Counter register CNTR: 3, 8-bit registers CNTRH, CNTRM, CNTRL**
  - **Found at addresses (PIT +$2E, $30, $32)**
  - **Address PIT + $2C has no real register but used as fake address for CNTR to complete a long word.**

```
PIT     EQU   $0FF000   Base Address of PI/T
PGCR    EQU   PIT       Port General Control Register
PSRR    EQU   PIT+2     Port service request register
PADDR   EQU   PIT+4     Data direction register A
PBDDR   EQU   PIT+6     Data direction register B
PCDDR   EQU   PIT+$08   Data direction register C
PIVR    EQU   PIT+$0A   Port Interrupt Vector register
PACR    EQU   PIT+$0C   Port A control register
PBCR    EQU   PIT+$0E   Port B control register
PADR    EQU   PIT+$10   Port A data register
PBDR    EQU   PIT+$12   Port B data register
PCDR    EQU   PIT+$18   Port C data register
PSR     EQU   PIT+$1A   Port status register
TCR     EQU   PIT+$20   Timer control register
TIVR    EQU   PIT+$22   Timer interrupt vector register
CPR     EQU   PIT+$24   Dummy address of preload register
CPRH    EQU   PIT+$26   Timer preload register high
CPRM    EQU   PIT+$28   Timer preload register middle
CPRL    EQU   PIT+$2A   Timer preload register low
CNTR    EQU   PIT+$2C   Dummy address of timer register
CNTRH   EQU   PIT+$2E   Timer register high
CNTRM   EQU   PIT+$30   Timer register middle
CNTRL   EQU   PIT+$32   Timer register low
TSR     EQU   PIT+$34   Timer status register
```

Addresses of Port Related Registers

Addresses of Timer Related Registers

68230 Registers Address Equates

Format of Timer Control Register (TCR)

TCR7 TCR6 TCR5	TCR4	TCR3	TCR2 TCR1	TCR0
Tout/TIACK* Control	Zero-detect Control	None	Clock Control	Timer Enable
Set function of port C lines including interrupt usage (PC3/Tout)	0 load from CPR 1 roll over on zero detect	Still none ;-)	Set source of timer clock Scaled by 32 or not	Bit 0 Disable 1 Enable

TCR Format for Different Timer Modes

Mode	TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0
1	1	X	1	0	0	00 or	1X	1
2	0	1	X	0	0	00 or	1X	1
3	1	X	1	1	0	00 or	1X	1
4	0	0	X	1	0	0	0	1
5	0	0	X	1	0	0	X	1
6	1	X	1	1	0	0	1	1
	Tout/TIACK* Control			ZD Control	None	Clock Control		Timer Enable

Mode 1 = Real-time clock
Mode 2 = Square wave generator
Mode 3 = Interrupt after timeout
Mode 4 = Elapsed time measurement
Mode 5 = Pulse counter
Mode 6 = Period measurement

Delay Subroutine Example Using 68230 Timer

- **The following subroutine DELAY can be called by a main program to introduce a delay in execution, no parameters are passed to DELAY:**
  - **Reset the timer.**
  - **Pre-load the timer with a value (determines delay).**
  - **Keep checking ZDS (busy looping) until the timer hits zero then return to calling program; no result is passed back.**

```
        ORG     $2000
DELAY   MOVE.B  #$00,TCR        Disable/Reset timer
        MOVE.L  #500000,D0      Load D0 with a very large value :-)
        LEA     CPR,A0          Load A0 with fake address of CPR
        MOVE.L  D0,(A0)         Preload the counter
        MOVE.B  #$01,TCR        Enable the timer TCR0 = 1
WAIT    BTST    #0,TSR          Check ZDS if done
        BNE     WAIT            Loop until counter hits zero
        RTS                     Done return to main program
        STOP    #$2700
```