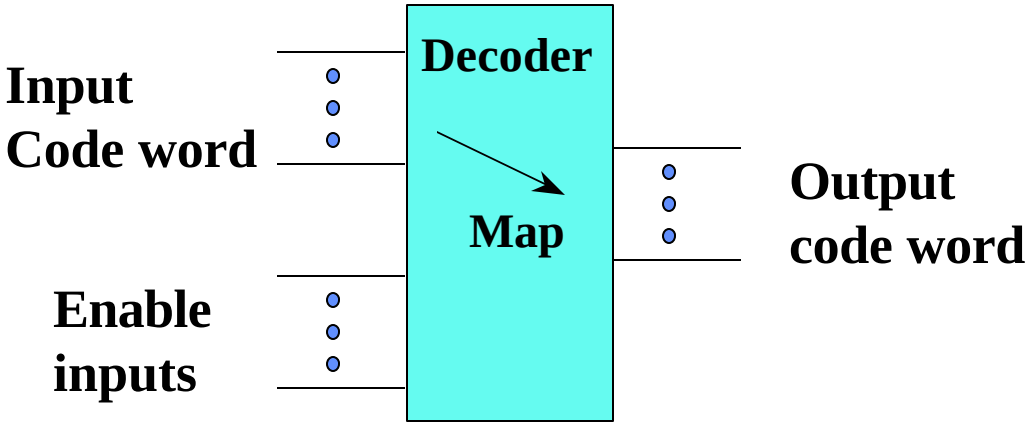
Combinational Logic Building Blocks

- **Decoders:**
  - Binary n-to-2^n decoders.
  - Implementing functions using decoders.
- **Encoders:**
  - 2^n -to-n binary decoders.
- **Three-State Buffers.**
- **Multiplexers.**
- **Demultiplexers**

Decoders

- **A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different.**
  e.g. n-to-2^n, BCD decoders.
- **Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word.**



Decoder Example: Seven-Segment Decoders

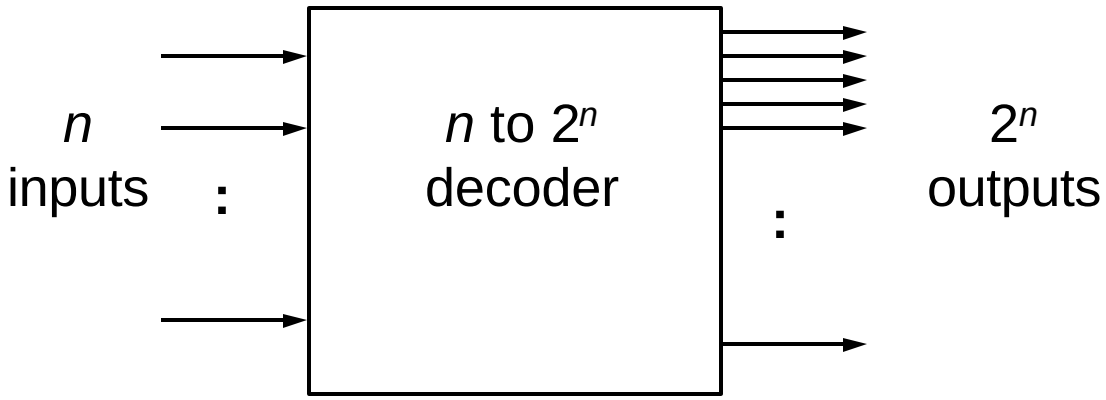
- A seven segment decoder has 4-bit BCD input and the seven segment display code as its output:
- In minimizing the circuits for the segment outputs all non-decimal input combinations (1010, 1011, 1100,1101, 1110, 1111) are taken as don't-cares

/Bl	D	C	B	A	a	b	c	d	e	f	g
0	x	x	x	x	0	0	0	0	0	0	0
1	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
1	0	0	1	0	1	1	0	1	1	0	1
1	0	0	1	1	1	1	1	1	0	0	1
1	0	1	0	0	0	1	1	0	0	1	1
1	0	1	0	1	1	0	1	1	0	1	1
1	0	1	1	0	0	0	1	1	1	1	1
1	0	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	0	0	1	1
1	1	0	1	0	0	0	0	1	1	0	1
1	1	0	1	1	0	0	1	1	0	0	1
1	1	1	0	0	0	1	0	0	0	1	1
1	1	1	0	1	1	0	0	1	0	1	1
1	1	1	1	0	0	0	0	1	1	1	1
1	1	1	1	1	0	0	0	0	0	0	0

-- don't care inputs --

Binary n-to-2^n Decoders

- **A binary decoder has n inputs and 2^n outputs.**
- **Only the output corresponding to the input value is equal to 1.**

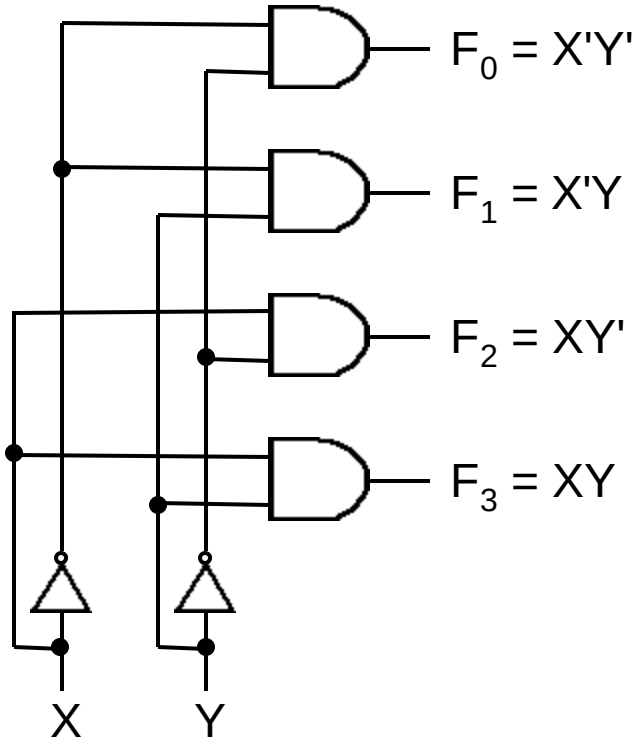


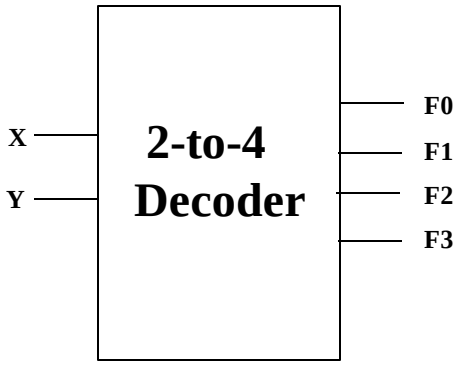
2-to-4 Binary Decoder

Truth Table:

X	Y	F_0	F_1	F_2	F_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- **From truth table, circuit for 2x4 decoder is:**
- **Note: Each output is a 2-variable minterm (**X'Y', X'Y, XY' **or** XY**)**

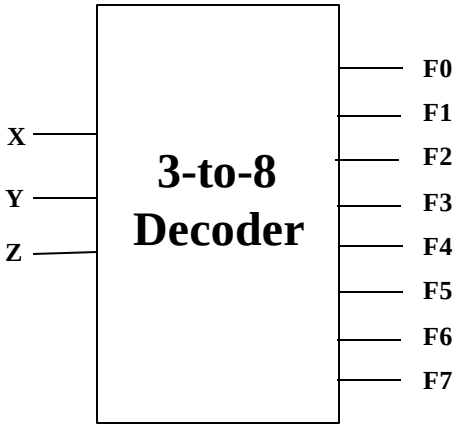


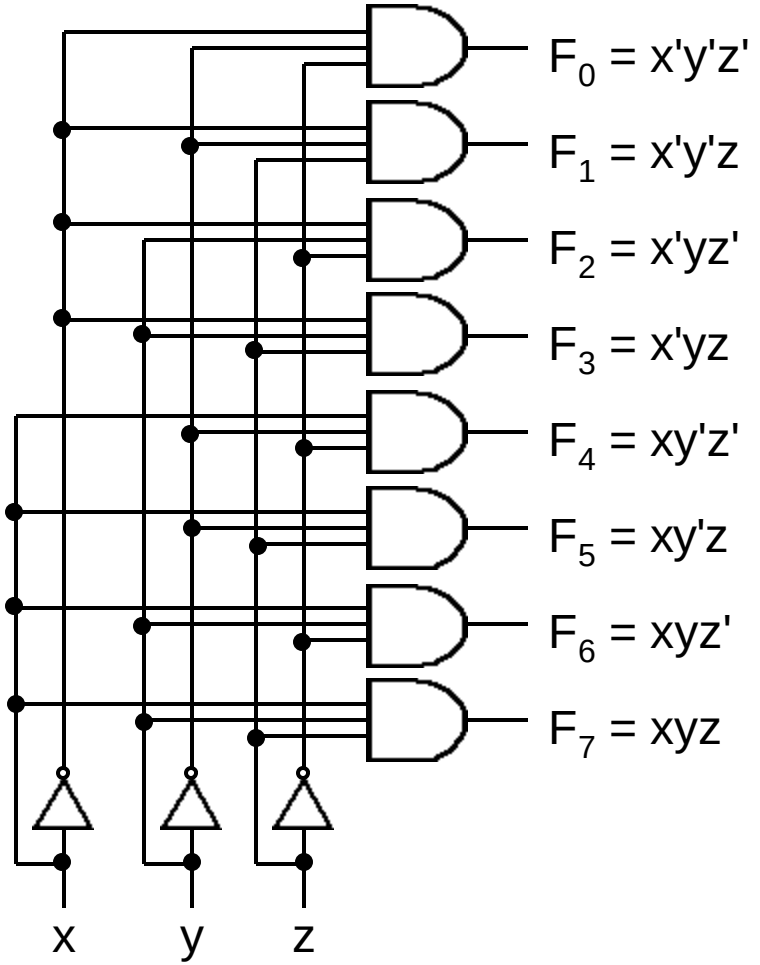


3-to-8 Binary Decoder

Truth Table:

x	y	z	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1





Implementing Functions Using Decoders

- **Any n-variable logic function, in canonical sum-of-minterms form can be implemented using a single n-to-2^n decoder to generate the minterms, and an OR gate to form the sum.**
  - The output lines of the decoder corresponding to the minterms of the function are used as inputs to the or gate.
- **Any combinational circuit with *n* inputs and *m* outputs can be implemented with an n-to-2^n decoder with *m* OR gates.**
- **Suitable when a circuit has many outputs, and each output function is expressed with few minterms.**

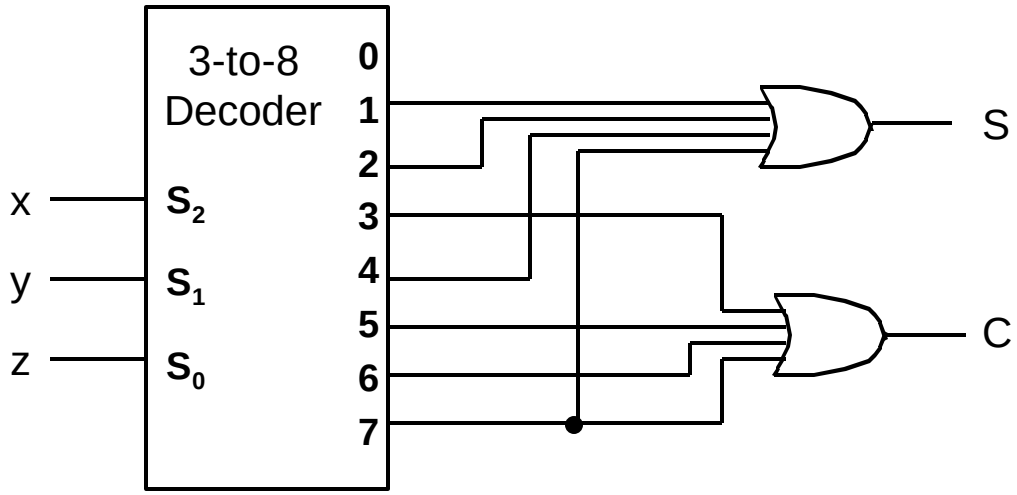
Implementing Functions Using Decoders

- **Example: Full adder**

$S(x, y, z) = \Sigma (1,2,4,7)$

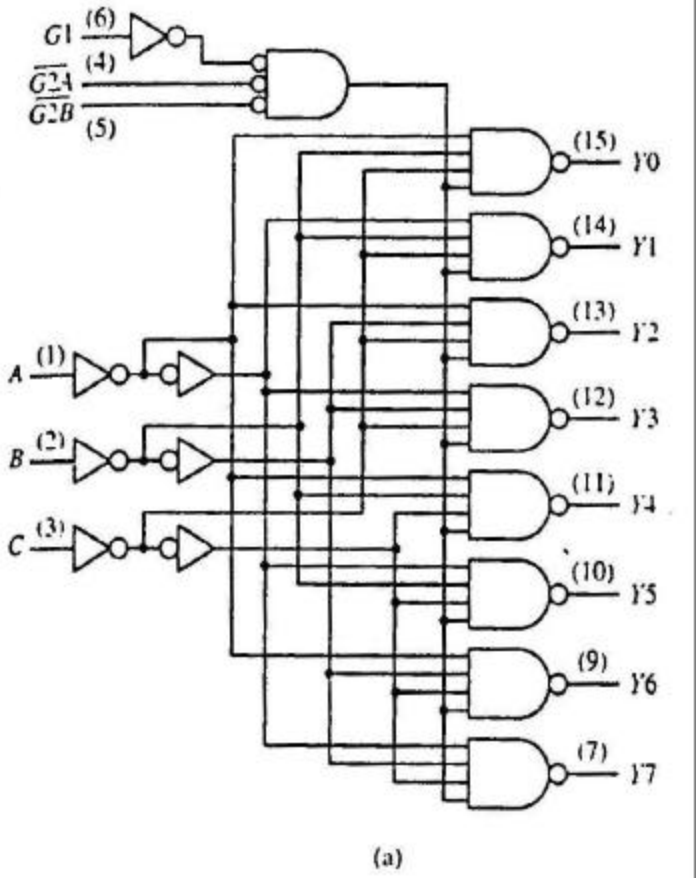
$C(x, y, z) = \Sigma (3,5,6,7)$

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

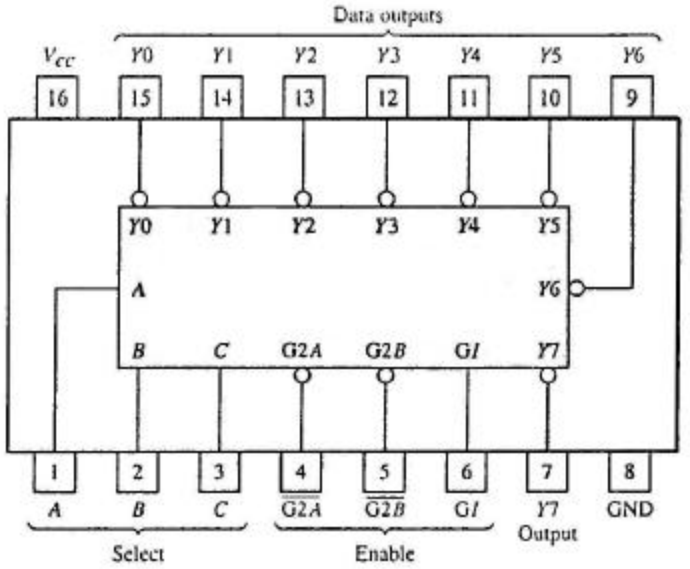


Standard MSI Binary Decoders Example

74138 (3-to-8 decoder)



(a)



(b)

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L
×	H	×	×	×	H	H	H	H	H	H	H	H
L	×	×	×	×	H	H	H	H	H	H	H	H

$\overline{G2}^* = \overline{G2A} + \overline{G2B}$

(c)

(a) Logic circuit.
(b) Package pin configuration.
(c) Function table.

Encoders

- If the a decoder's output code has fewer bits than the input code, the device is usually called an encoder.

  e.g. 2^n-to-n, priority encoders.

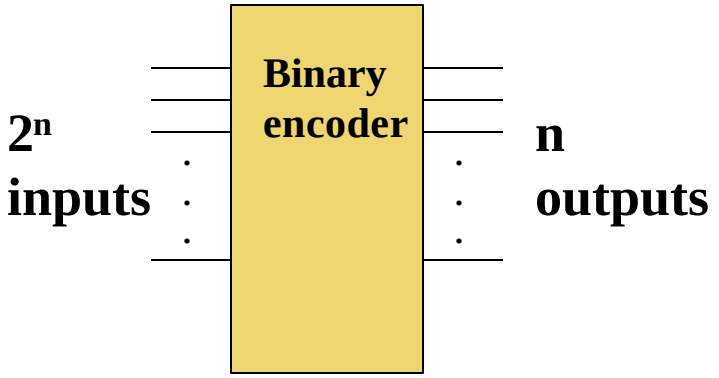
- The simplest encoder is a 2^n-to-n binary encoder, where it has only one of 2^n inputs = 1 and the output is the n-bit binary number corresponding to the active input.

- For an 8-to-3 binay encoder with inputs I0-I7 the logic expressions of the outputs Y0-Y2 are:

$$Y0 = I1 + I3 + I5 + I7$$

$$Y1 = I2 + I3 + I6 + I7$$

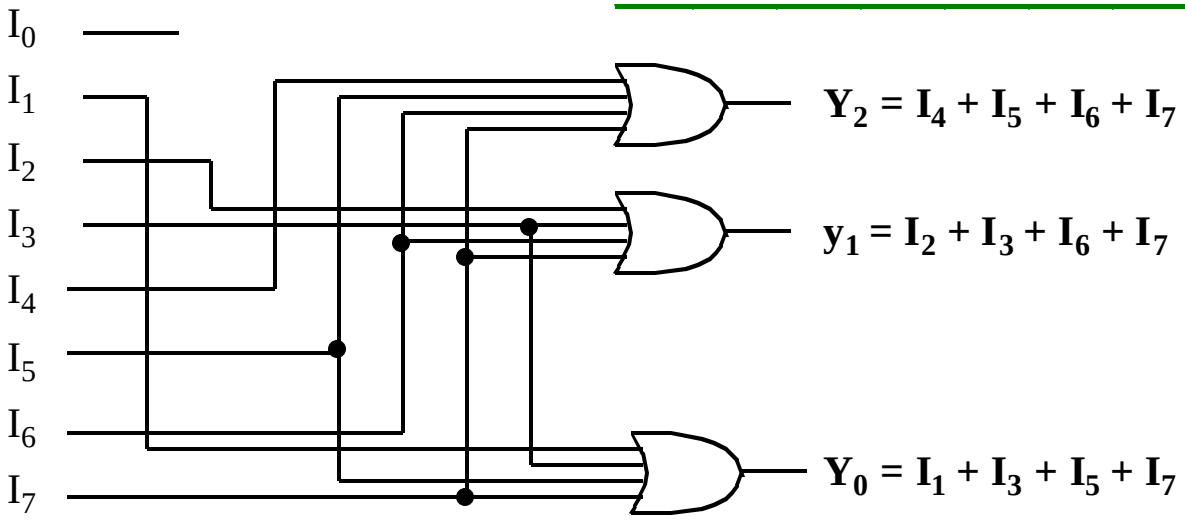
$$Y2 = I4 + I5 + I6 + I7$$



8-to-3 Binary Encoder

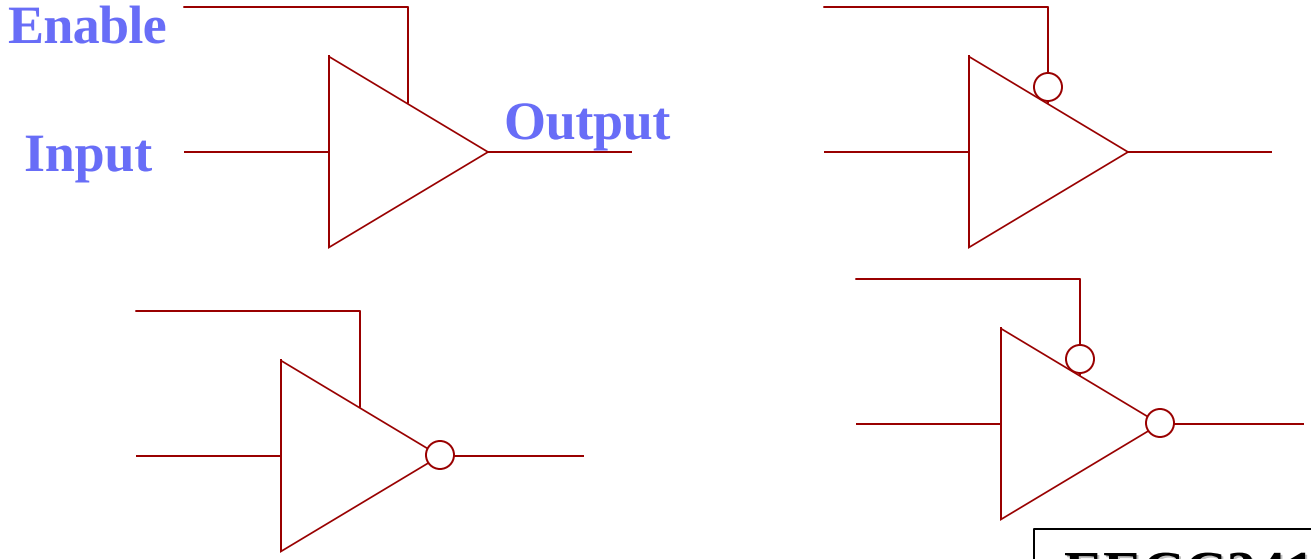
At any one time, only one input line has a value of 1.

Inputs								Outputs		
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	y_2	y_1	y_2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



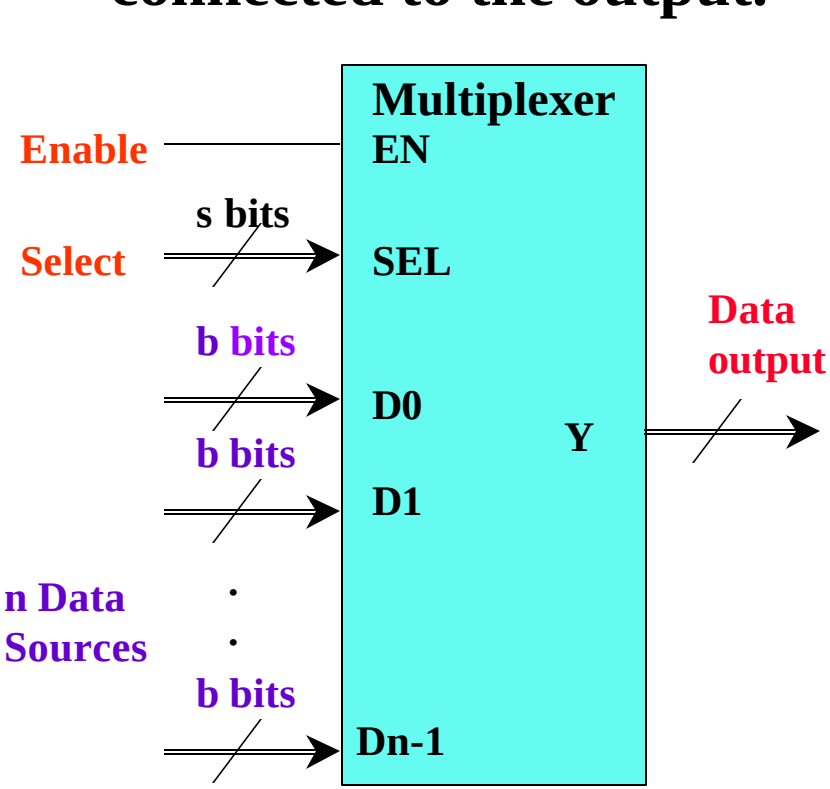
Three State (Tri-State) Buffers

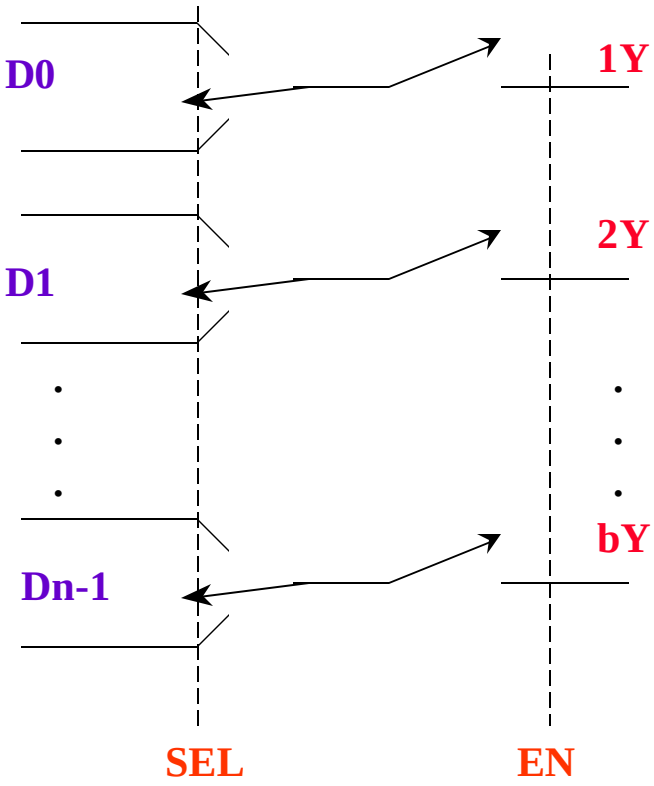
- Three state buffers are CMOS and TTL devices whose outputs may be in one of three states: 0, 1 or Hi-Z (high impedance, or floating state.
- Have an extra input called "output enable" or "output disable".
- When enables the device transmits the input value or its complement to the output.



Multiplexers

- A multiplexer (MUX) is a digital switches which connects data from one of n sources to the output.
- A number of select inputs determine which data source is connected to the output.



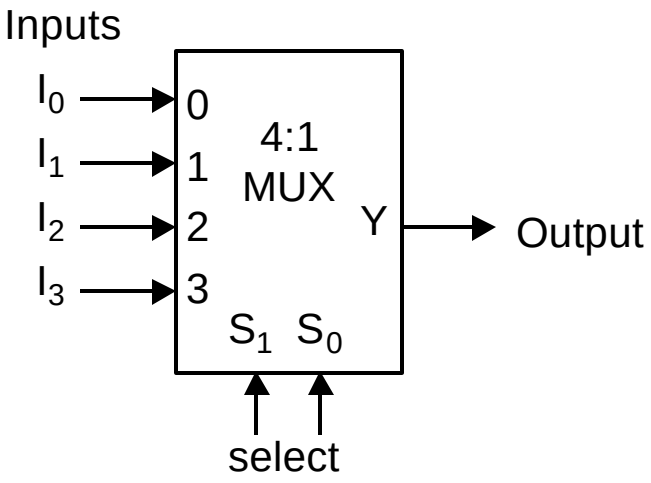


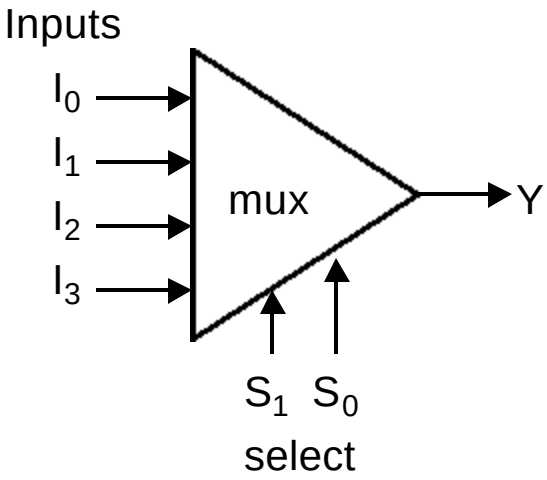
4-to-1 MUX

Truth table for a 4-to-1 multiplexer:

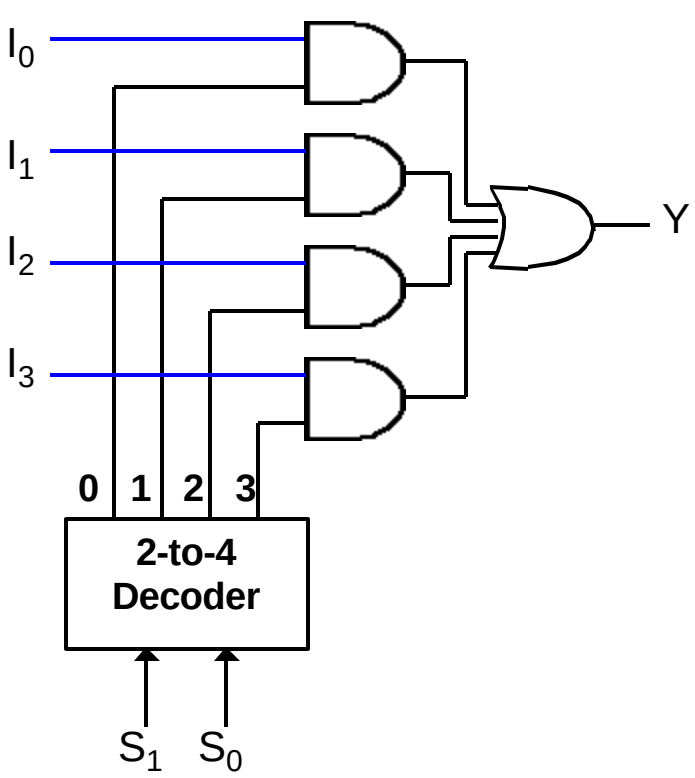
I_0	I_1	I_2	I_3	S_1	S_0	Y
d_0	d_1	d_2	d_3	0	0	d_0
d_0	d_1	d_2	d_3	0	1	d_1
d_0	d_1	d_2	d_3	1	0	d_2
d_0	d_1	d_2	d_3	1	1	d_3

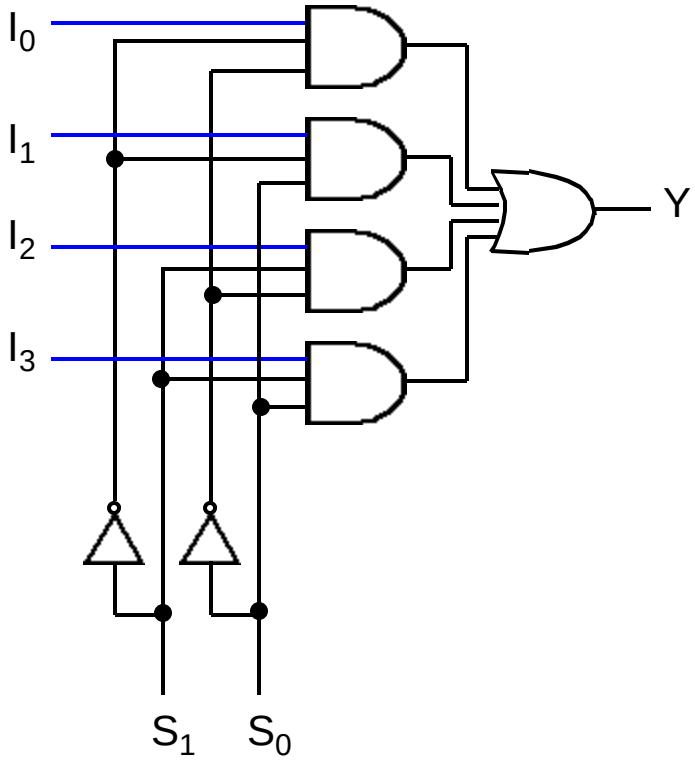
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3





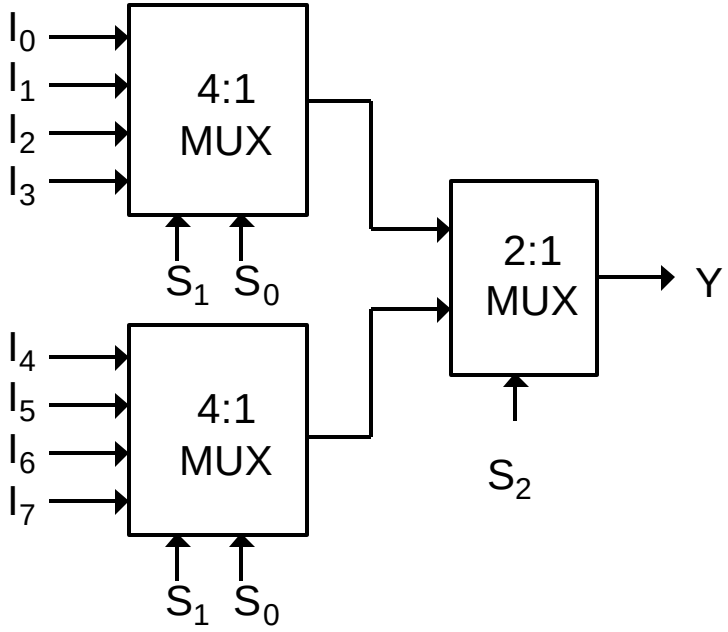
4-to-1 MUX Circuit





Larger Multiplexers

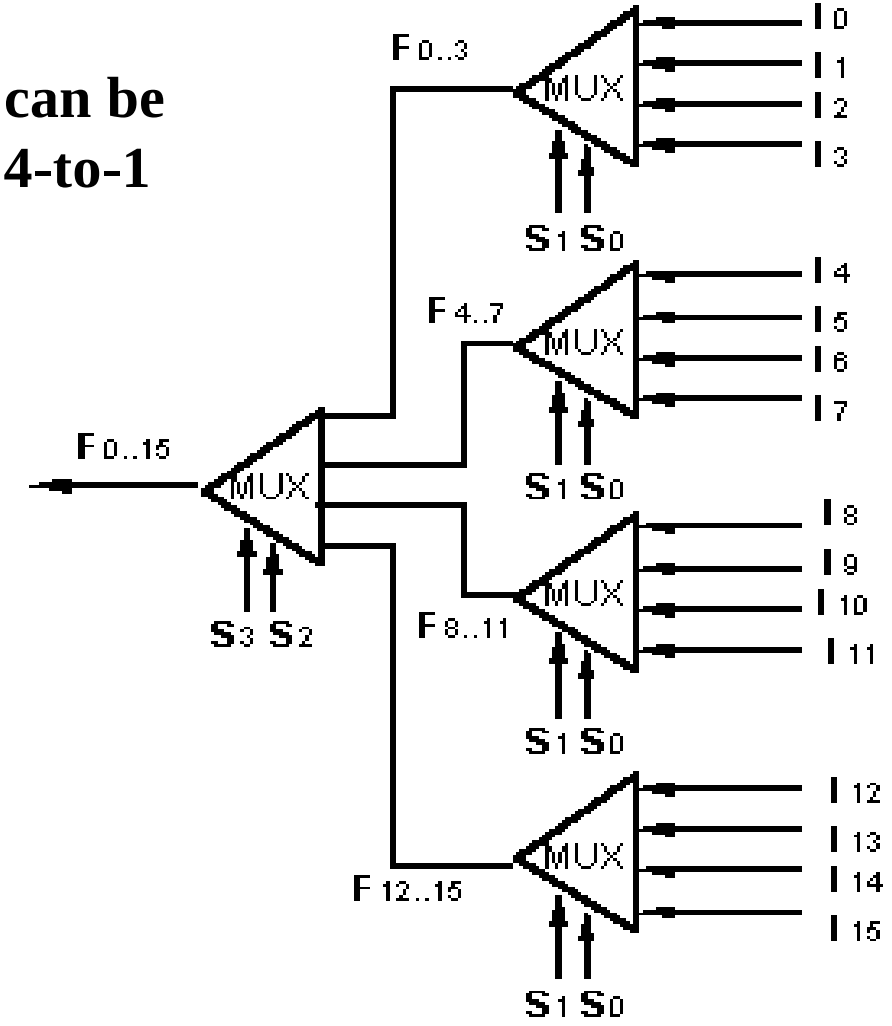
- **Larger multiplexers can be constructed from smaller ones.**
- **An 8-to-1 multiplexer can be constructed from smaller multiplexers as shown:**



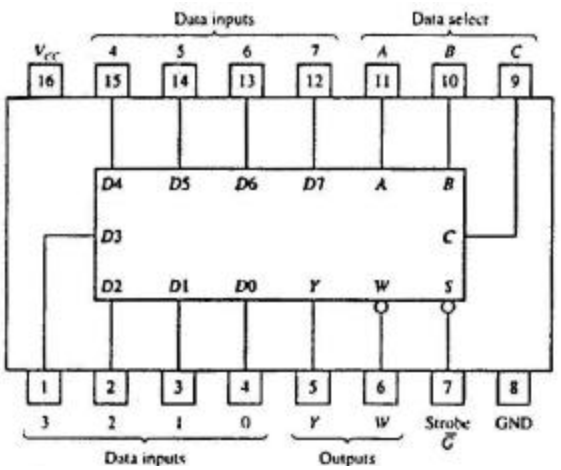
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

Larger Multiplexers

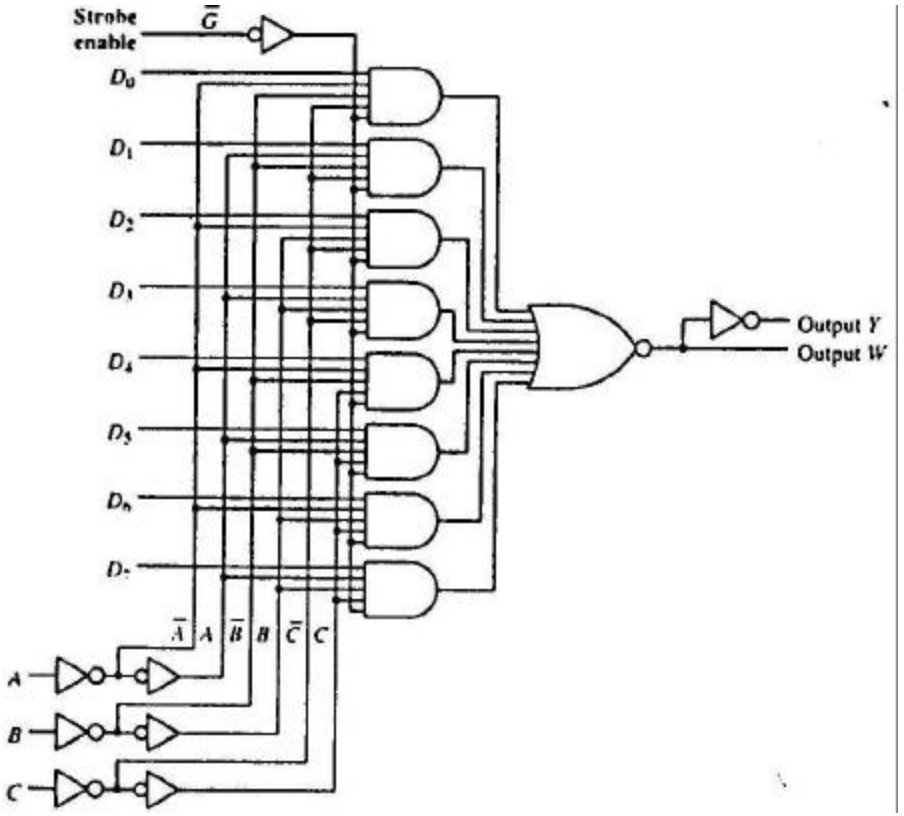
- **A 16-to-1 multiplexer can be constructed from five 4-to-1 multiplexers:**



Standard MSI Multiplexer Example



74151A 8-to-1 multiplexer.

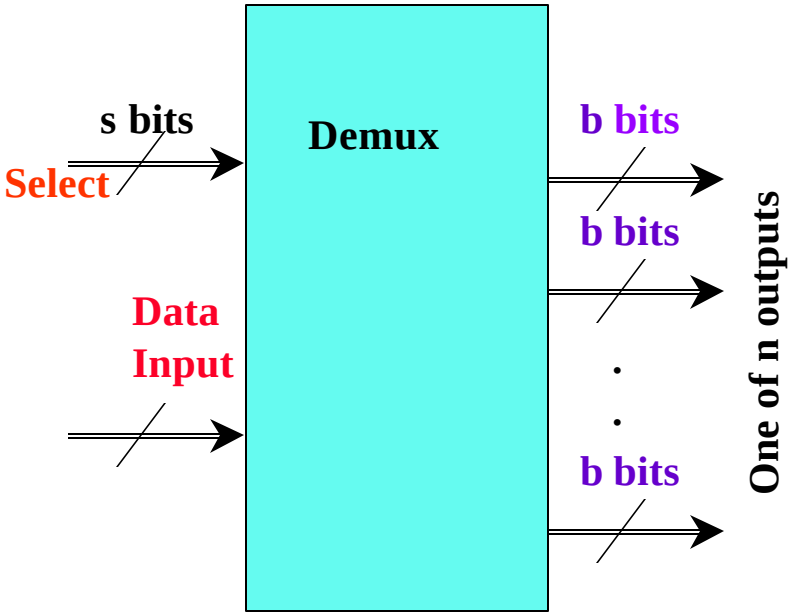


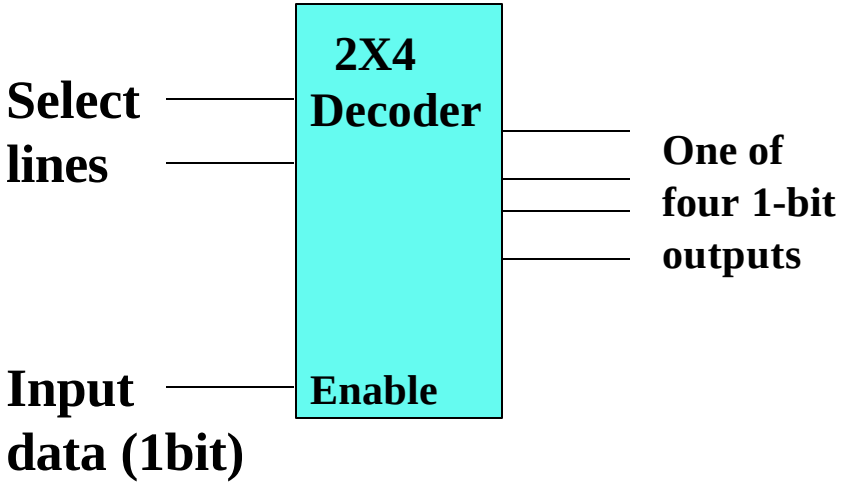
Inputs				Outputs	
Select			Strobe		
C	B	A	$\bar{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

(b)

Demultiplexers

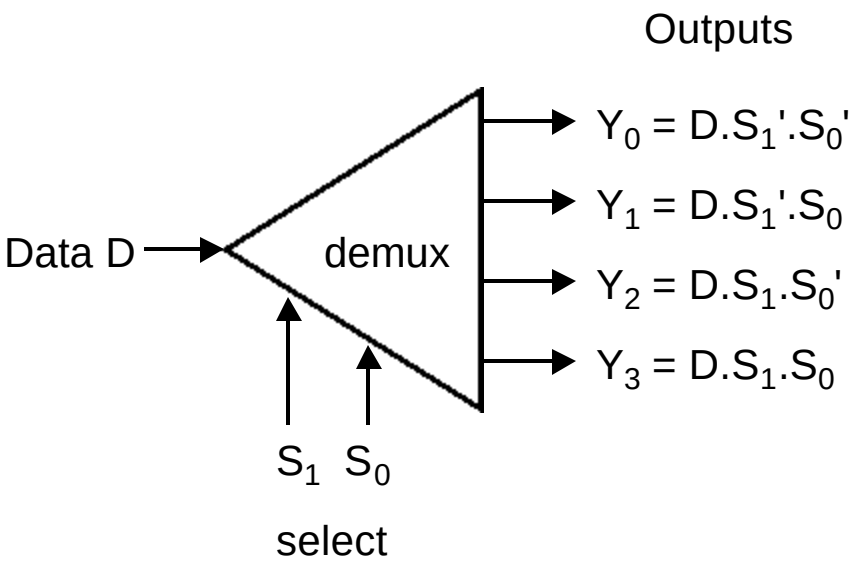
- Digital switches to connect data from one input source to one of n outputs.
- Usually implemented by using n-to-2^n binary decoders where the decoder's enable line is used for data input of the demultiplexer.



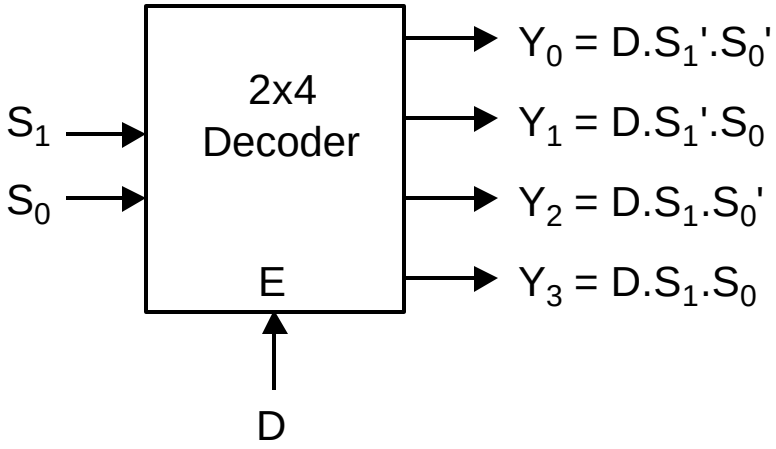


1-bit 4-output demultiplexer using a 2x4 binary decoder.

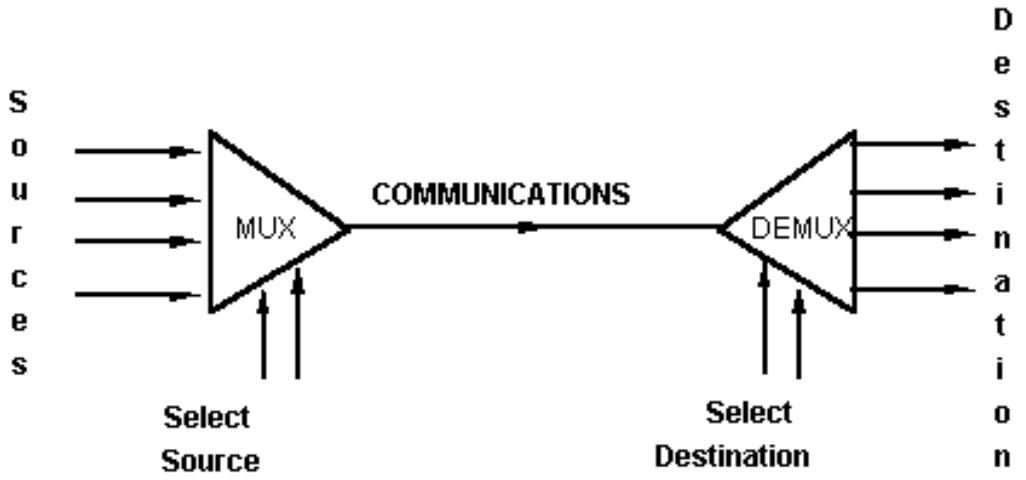
1-to-4 Demultiplexer



S_1	S_o	Y_0	Y_1	Y_2	Y_3
0	0	D	0	0	0
0	1	0	D	0	0
1	0	0	0	D	0
1	1	0	0	0	D



Mux-Demux Application Example



This enables sharing a single communication line among a number of devices.
At any time, only one source and one destination can use the communication line.