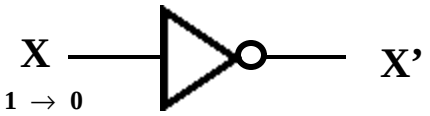
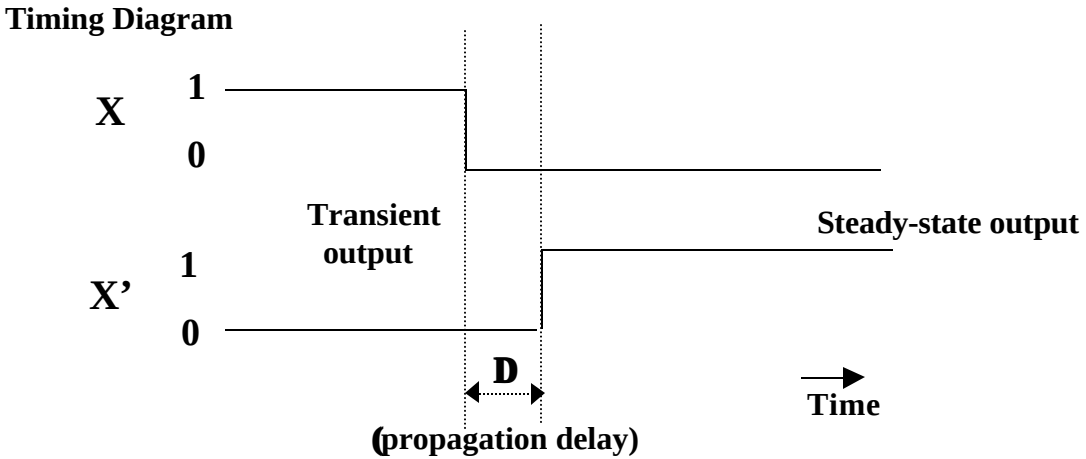
Combinational Logic Circuit Transient Vs. Steady-state Output

- **Gate propagation delay: The time between an input change and the corresponding change of the output.**
- **Circuit steady-state output: The output is evaluated when the inputs have been stable for a long time relative to the gate delays.**
- **Circuit transient output behavior: The circuit output when one or more inputs change values.**
- **Example: For an inverter with propagation delay, D when input changes from 1 to 0:**

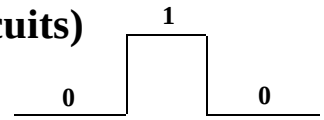




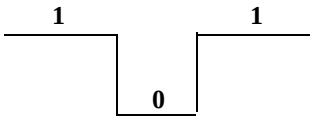
- **The circuit analysis done so far ignores propagation delays and considers only steady-state output when all propagation delays have completed though all the circuit gates.**

Combinational Logic Hazards

- **Output glitch: A momentary unexpected transient output change (short pulse) when an input changes and usually caused by gate propagation delays.**
- **Hazards: A hazard exists in a combinational circuit when it produces an output glitch when one or more inputs change.**
- **Types of combinational logic hazards:**
- **Static Hazards:**
  - **Static-1 Hazard: The output should be 1 but goes momentary to 0 as a result of an input change. (possible in AND-OR circuits)**
  - **Static-0 Hazard: The output should be 0 but goes momentary to 1 as a result of an input change. (possible in OR-AND circuits)**

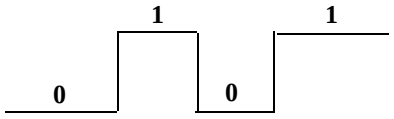


Static-0 Hazard



Static-1 Hazard

- **Dynamic Hazards: The output changes more than once as a result of a single input change (impossible in 2-level circuits).**



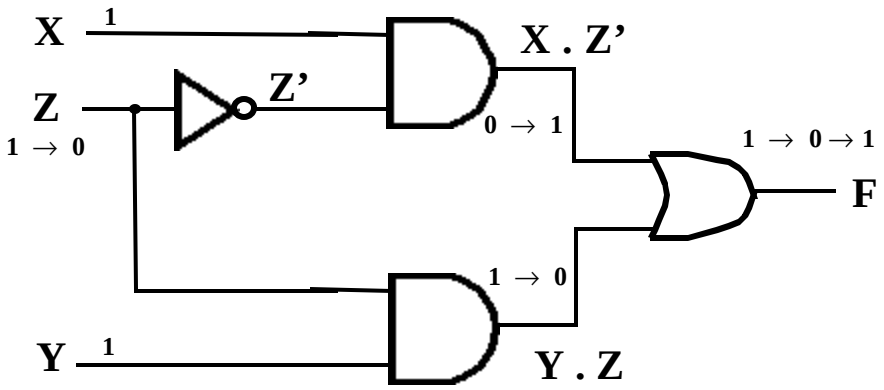
Dynamic Hazard Example

- **Static hazards can be detected and eliminated for 2-level logic circuits using K-maps.**

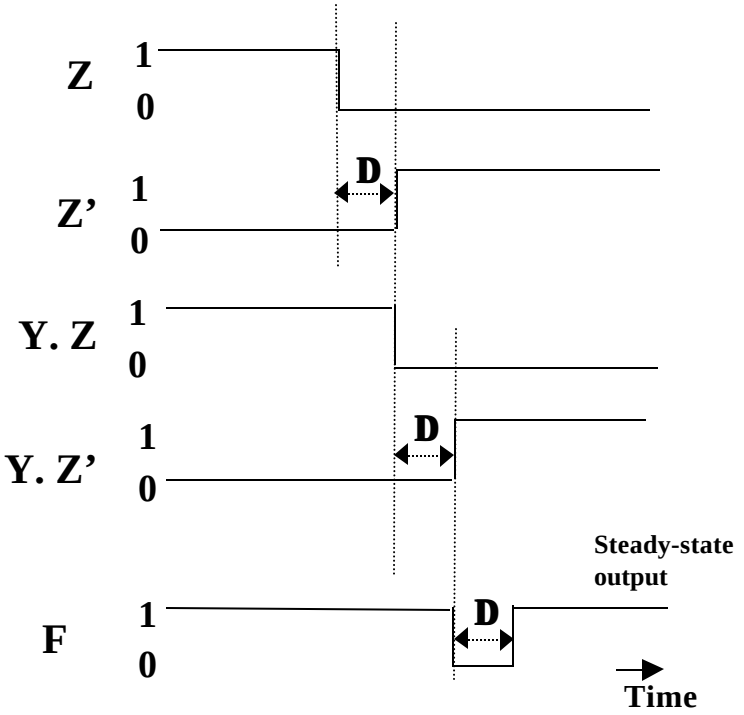
Example: Circuit with Static-1 Hazard

- **A static-1 hazard exists in the following AND-OR circuit when X = 1, Y = 1 and Z changes from 1 to 0 (assume all gates have propagation delay D):**

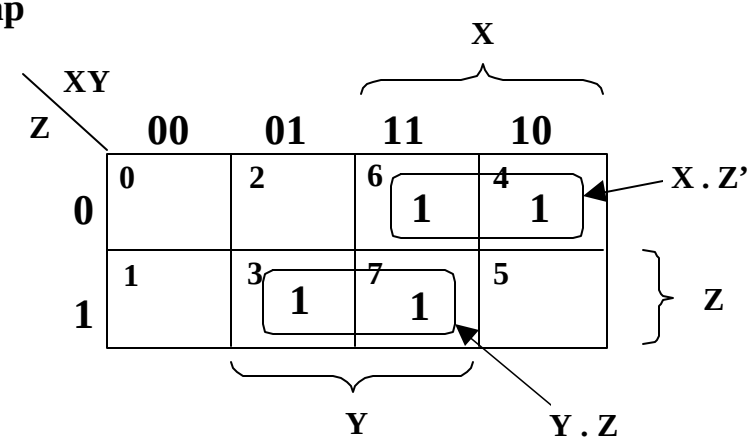
Circuit



Timing Diagram

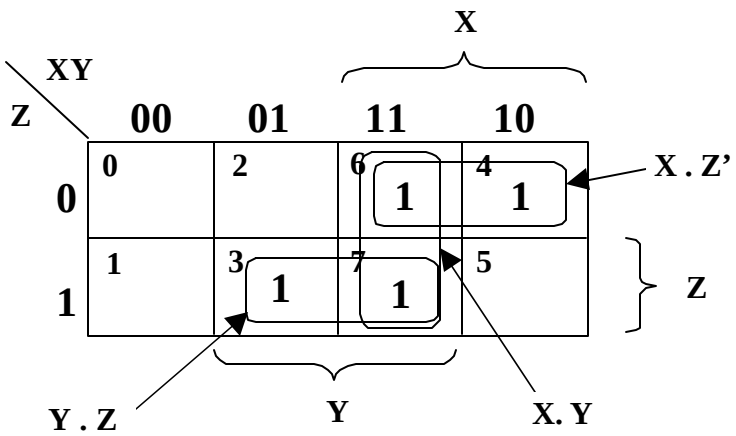


K-map

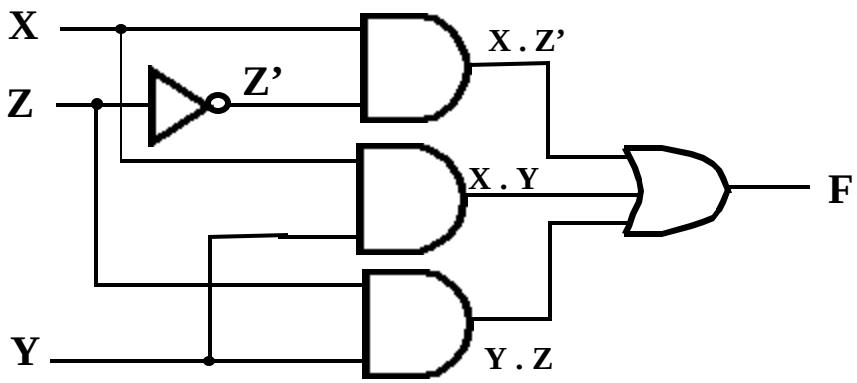


Eliminating Static-1 Hazards Using K-maps

- A static-1 hazard occurs in AND-OR circuits when an input variable and its complement are connected to two different AND gates.
- Static-1 hazards are found using k-maps by finding adjacent 1 cells that are covered by different product terms.
- To eliminate static-1 hazards, additional product terms (prime implicants) are needed to cover such cells thus covering the transition of the variable causing the hazard.
- For in the previous example the static-1 hazard is eliminated by including the additional product term X . Y



Circuit with static-1 hazard eliminated



New F = X . Z' + Y . Z + X. Y

Eliminating Static-0 Hazards Using K-maps

- **A static-0 hazard occurs in OR-AND circuits when an input variable and its complement are connected to two different OR gates.**
- **The procedure to find and eliminate static-0 hazards using K-maps is done in a dual way to finding static-1 hazards.**
- **Static-0 hazards are found using k-maps by finding adjacent 0 cells that are covered by different sum terms.**
- **To eliminate static-0 hazards, additional sum terms (prime implicates) are needed to cover such cells thus covering the transition of the variable causing the hazard.**