Memory Devices

• **Read Only Memory (ROM)**
  – Structure of diode ROM
  – Types of ROMs.
  – ROM with 2-Dimensional Decoding.
  – Using ROMs for Combinational Logic

• **Read/Write Memory**

  *(Random Access Memory, RAM):*
  – Types of RAM:
    • Static RAM (SRAM)
    • Dynamic RAM (DRAM)
  – SRAM Timing
  – DRAM Timing
Read-Only Memory (ROM)

- A combinational circuit with \( n \) inputs and \( b \) outputs:

\[
\begin{align*}
\text{Address inputs} & \quad n \\
A(n-1, \ldots, 0) & \quad 2^n \times b \\
\text{ROM} & \\
\text{Data outputs} & \quad b \\
D(b-1, \ldots, 0) &
\end{align*}
\]

- Programmable — values determined by user
- Nonvolatile — contents retained without power
- Uniform (Random) Access — delay is uniform for all addresses
Read-Only Memory (ROM)

- **Two views of ROM:**
  - ROM stores $2^n$ words of $b$ bits each, or
  - ROM stores an $n$-input, $b$-output truth table

<table>
<thead>
<tr>
<th>n = 2</th>
<th>b = 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example:</td>
<td>A1 A0</td>
</tr>
<tr>
<td>0 0</td>
<td>0 1 0 1</td>
</tr>
<tr>
<td>0 1</td>
<td>1 1 1 1</td>
</tr>
<tr>
<td>1 0</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>1 1</td>
<td>1 0 0 0</td>
</tr>
</tbody>
</table>
Internal Structure of 4×4 Diode ROM

2 to 4 Decoder

A1
A0

/w0
/w1
/w2
/w3

Diode
No Diode

R0 R1 R2 R3

+5 V

0101 ← 1 of n Word Lines
1111
0001
1000

Bit Lines

D0
D1
D2
D3
Types Of ROMs

- **Mask ROM**
  - Connections made by the semiconductor vendor
  - Expensive setup cost, Several weeks for delivery. High volume only
  - Bipolar or MOS technology

- **PROM**
  - Programmable ROM
  - Vaporize (blow) fusible links with PROM programmer using high voltage/current pulses
  - Bipolar technology
  - One-time programmable

- **EPROM**
  - Erasable Programmable ROM
  - Charge trapped on extra “floating gate” of MOS transistors
  - Exposure to UV light removes charge. Limited number of erasures (10-100)

- **EEPROM (E²ROM)**
  - Electrically Erasable ROM
  - Not RAM (relatively slow charge/discharge)
  - limited number of charge/discharge cycles (10,000)

- **Flash Memory**
  - Electronically erasable in blocks
  - 100,000 erase cycles
  - Simpler and denser than EEPROM
## ROM Type Summary

<table>
<thead>
<tr>
<th>Type</th>
<th>Technology</th>
<th>Read Cycle</th>
<th>Write Cycle</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>NMOS, CMOS</td>
<td>20-200 ns</td>
<td>4 weeks</td>
<td>Write once; low power</td>
</tr>
<tr>
<td>Mask ROM</td>
<td>Bipolar</td>
<td>&lt;100 ns</td>
<td>4 weeks</td>
<td>Write once; high power; low density</td>
</tr>
<tr>
<td>PROM</td>
<td>Bipolar</td>
<td>&lt;100 ns</td>
<td>5 minutes</td>
<td>Write once; high power; no mask charge</td>
</tr>
<tr>
<td>EPROM</td>
<td>NMOS, CMOS</td>
<td>25-200 ns</td>
<td>5 minutes</td>
<td>Reusable; low power; no mask charge</td>
</tr>
<tr>
<td>EEPROM</td>
<td>NMOS</td>
<td>50-200 ns</td>
<td>10 μs/byte</td>
<td>10,000 writes/location limit</td>
</tr>
<tr>
<td>FLASH</td>
<td>CMOS</td>
<td>25-200 ns</td>
<td>10 μs/block</td>
<td>100,000 erase cycles</td>
</tr>
</tbody>
</table>
Internal Structure of Transistor ROM

- Replace diodes with MOS transistors
- Change decoder to active-high outputs

Transistor $\rightarrow$ 1
No transistor $\rightarrow$ 0
EPROM and EEPROM Structure

Floating gate

Active-high word lines

Active-low bit lines

V\textsubscript{DD}
64 x 1 ROM with 2-Dimensional Decoding

3 to 8 Decoder

A5
\[\downarrow\]
A3

A2
\[\downarrow\]
A0

8 x 8 Diode Array

0
7

8 to 1 mux

D0

Almost square chip
Internal $2^n \times b$ ROM Structure
# Using ROMs for Combinational Logic

Example A 3-input, 4-output combinational logic function:

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_2 )</td>
<td>( A_1 )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Function: 2-to-4 Decoder with Polarity Control

\( A_2 = \) Polarity \((0 = \text{active Low}, 1 = \text{active High})\)

\( A_1, A_0 = I_1, I_0 \) \((2\text{-bit input})\)

\( D_3...D_0 = Y_3...Y_0 \) \((4\text{-bit decoded output})\)
Read/Write Memory (RWM / RAM)

- RWM = RAM (Random Access Memory)
- Highly structured like ROMs
- Can store and retrieve data at (relatively) the same speed

- Static RAM (SRAM) retains data in latches (while powered)
- Dynamic RAM (DRAM) stores data as capacitor charge; all capacitors must be recharged periodically (refresh).

- Volatile Memory: Both Static and Dynamic RAM
- Nonvolatile Memory: Data retained when power lost
  = ROMs, NVRAM (w/battery), Flash Memory
Basic Structure of SRAM

- Address/Control/Data Out lines like a ROM (Reading)
  + Write Enable (WE) and Data In (DIN) (Writing)
One Bit of SRAM

- SEL and WR asserted \(\rightarrow\) IN data stored in D-latch (Write)
- SEL only asserted \(\rightarrow\) D-latch output enabled (Read)
- SEL not asserted \(\rightarrow\) No operation
SRAM Timing

• During READ, outputs are combinational functions of ADDR, CS, OE (like ROM)
  – Inputs can freely change without problems (except for propagation delay from last input change to output)

• During WRITE, data stored in latches, NOT FF’s.
  – Thus, Setup & Hold on Data IN relative to trailing edge of /WR

• Address must be stable
  – for setup time before /WR asserted, and
  – for hold time after /WR deasserted
    • to prevent “spraying” data to multiple rows

• /WR asserted when BOTH /CS and /WE asserted
• /WR deasserted when EITHER /CS or /WE deasserted
READ Timing (SRAM)

Primary Spec for SRAMs

\[ \max(t_{AA}, t_{ACS}) \]
WRITE Timing (SRAM)

- **ADDR**: stable
- **/CS**: stable
- **/WE**: (WE-controlled write)
  - $t_{CSW}$
- **DIN**: valid
- **/WE**: (CS-controlled write)
  - $t_{AS}$
  - $t_{CSW}$

- **t_DS**
- **t_DH**
- **t_WP**
- **t_AH**
Example: 16 x 1 SRAM $\rightarrow$ 4 x 4 Array
64K x 8 RAM with 2-D Decoding

A

9

9 to 512 Decoder

512

512

512

512

512

512

512

Mux

Array

D0 D1 D7
Classic DRAM Organization

- Row and Column Address together:
  - Select 1 bit at a time

Each intersection represents a 1-T DRAM Cell

bit (data) lines

word (row) select

row decoder

row address

Column Selector & I/O Circuits

Column Address

data

RAM Cell Array
Logical Diagram of A Typical DRAM

° Control Signals (RAS_L, CAS_L, WE_L, OE_L) are all active low

° Din and Dout are combined (D):
  • WE_L is asserted (Low), OE_L is disasserted (High)
    - D serves as the data input pin
  • WE_L is disasserted (High), OE_L is asserted (Low)
    - D is the data output pin

° Row and column addresses share the same pins (A)
  • RAS_L goes low: Pins A are latched in as row address
  • CAS_L goes low: Pins A are latched in as column address
64K x 1 DRAM

- Row decoder
- 256 x 256 array
- Row register, Data mux/demux

1-bit DRAM cell

- Word line
- Bit line

- ADDR
- /RAS
- /CAS
- /WE

- Col ADDR
- Control

- 64K x 1 DRAM
  - ADDR
  - Din
  - RAS
  - CAS
  - WE
  - Dout
Standard Asynchronous DRAM Read Timing

$t_{RAC}$: Minimum time from RAS (Row Access Strobe) line falling to the valid data output. Usually quoted as the nominal speed of a DRAM chip. For a typical 4Mb DRAM $t_{RAC} = 60$ ns

$t_{RC}$: Minimum time from the start of one row access to the start of the next. $t_{RC} = 110$ ns for a 4Mbit DRAM with a $t_{RAC}$ of 60 ns
Four Key DRAM Timing Parameters

• $t_{RAC}$: Minimum time from RAS (Row Access Strobe) line falling to the valid data output.
  – Usually quoted as the nominal speed of a DRAM chip
  – For a typical 4Mb DRAM $t_{RAC} = 60$ ns

• $t_{RC}$: Minimum time from the start of one row access to the start of the next.
  – $t_{RC} = 110$ ns for a 4Mbit DRAM with a $t_{RAC}$ of 60 ns

• $t_{CAC}$: minimum time from CAS (Column Access Strobe) line falling to valid data output.
  – 15 ns for a 4Mbit DRAM with a $t_{RAC}$ of 60 ns

• $t_{PC}$: minimum time from the start of one column access to the start of the next.
  – About 35 ns for a 4Mbit DRAM with a $t_{RAC}$ of 60 ns
Simplified Asynchronous DRAM Read Timing

Source: http://arstechnica.com/paedia/r/ram_guide/ram_guide.part2-1.html
Modern DRAM Timing

• **Fast-Page Mode, FPM DRAM (One RAS, multiple CAS)**
  – Multiple bits of a row can be written before rewrite
  – Complex control, but much faster

• **Extended Data Out, EDO DRAM (One RAS, multiple CAS)**
  – Latches the column address so that the next address can be prepared *while* the output is read
  – Saves ~10ns/read, and increase of 10-15%
  – Even more complex control.

• **SDRAM - Synchronous DRAM**
  – Unlike normal DRAM, SDRAM is clocked.
  – Multiple signals and banks (row-address registers) allow “pipelined” operation
Page Mode DRAM: Motivation

° Regular DRAM Organization:
  - N rows x N column x M-bit
  - Read & Write M-bit at a time
  - Each M-bit access requires a RAS / CAS cycle

° Fast Page Mode DRAM
  - N x M “register” to save a row
Fast Page Mode DRAM: Operation

- **Fast Page Mode DRAM**
  - $N \times M$ "SRAM" to save a row

- **After a row is read into the register**
  - Only CAS is needed to access other M-bit blocks on that row
  - RAS_L remains asserted while CAS_L is toggled

![Diagram of Fast Page Mode DRAM Operation](image-url)
Simplified Asynchronous Fast Page Mode (FPM) DRAM Read Timing

Typical timing at 66 MHZ: 5-3-3-3
For bus width = 64 bits = 8 bytes  Max. Bandwidth = 8 x 66 / 3 = 176 Mbytes/sec

Source: http://arstechnica.com/paedia/r/ram_guide/ram_guide.part2-1.html
Extended Data Out DRAM operates in a similar fashion to Fast Page Mode DRAM except the data from one read is on the output pins at the same time the column address for the next read is being latched in.

EDO Read

EDO DRAM speed rated using tRAC ~ 40-60ns

Typical timing at 66 MHZ: 5-2-2-2
For bus width = 64 bits = 8 bytes Max. Bandwidth = 8 x 66 / 2 = 264 Mbytes/sec

Source: http://arstechnica.com/paedia/r/ram_guide/ram_guide.part2-1.html
Synchronous
Dynamic RAM (SDRAM) Organization

SDRAM speed is rated at max. clock speed supported:
66MHZ = PC66
100MHZ = PC100
133MHZ = PC133
150MHZ = PC150
Typical timing at 133 MHZ (PC133 SDRAM) : 4-1-1-1
For bus width = 64 bits = 8 bytes     Max. Bandwidth = 133 x 8 = 1064 Mbytes/sec

RAM Summary

SRAM:
• Fast
• Simple Interface
• Moderate bit density (4 gates → 4 to 6 transistors)
• Moderate cost/bit

DRAM (Dynamic RAM):
• moderate speed
• complex interface
• High bit density (1 transistor cell)
• Low cost/bit

Small systems or very fast applications (cache memory)

Large Memories: PC’s Mainframes