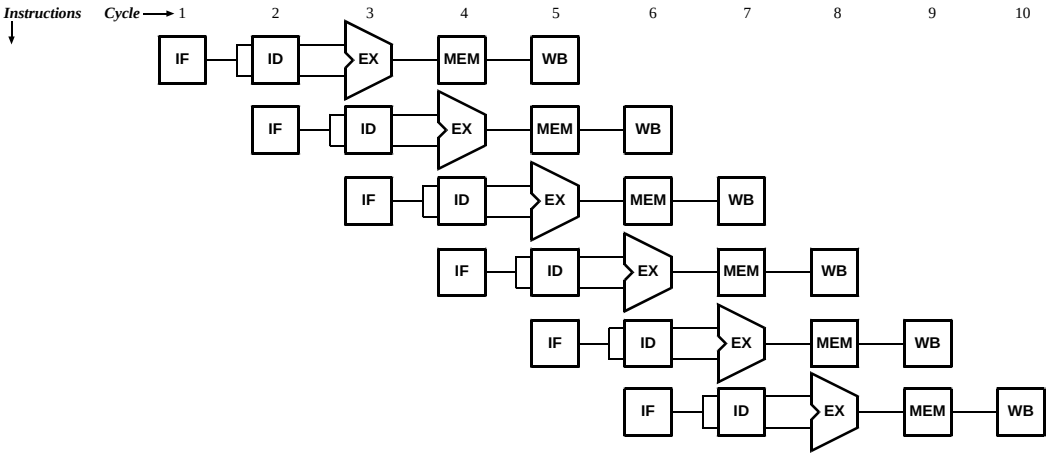
Computer Organization (0306-550) - Winter 2012

Homework Assignment #4 - Due Tuesday February 5

1. **Using a timing diagram similar to the figure below, indicate the forwarding paths used and possible stalls needed to execute these instructions on the MIPS pipeline with forwarding (MIPS pipeline version 2 or 3).**

```
add    $3,  $4, $6
add    $5,  $3, $2
lw     $7,  100($5)
add    $8,  $7, $2
```



2. **Consider executing the following code on the MIPS pipelined datapath version 2 with forwarding (4th Edition Figure 4.60 page 375 - 3rd Edition Figure 6.36 page 416)**

```
add    $2,  $3, $1
add    $4,  $3, $5
add    $5,  $3, $7
add    $7,  $6, $1
add    $8,  $2, $6
```

a) **During the fifth cycle of execution, which registers will be read, and which register will be written?**

b) **During the fifth cycle of execution, what is the forwarding unit doing? If any comparisons are made, list them.**

c) **During the fifth cycle of execution, what is the hazard detection unit doing? If any comparisons are made, list them.**

3. **Consider a 1,000-instruction program of alternating `lw` and `add` instructions: `lw`, `add`, `lw`, `add`, etc. The `add` instruction depends (and only depends) on the `lw` instruction immediately before it. The `lw` instruction depends (and only depends) on the `add` immediately before it.**

a) **If the code is executed on a MIPS pipelined datapath with forwarding (pipeline version 2 or 3), what would be its CPI?**

b) **If the code is executed on a MIPS pipelined datapath without forwarding (pipeline version 1), what would be its CPI?**

4. **For the following MIPS code:**

```
loop:   lw    $1,  0($2)
        lw    $1,  8($1)
        add   $1,  $1, $8
        lw    $3,  0($4)
        lw    $3,  12($3)
        add   $1,  $1,  $3
        addi  $2,  $2,  4
        addi  $4,  $4,  4
        sw    $1,  0($5)
        sub   $6,  $7,  $2
        addi  $5,  $5,  4
        bne   $6,  $0,  loop
```

Assuming that initially: $2 = $7 - 26000 Find (1) the total number of cycles, (2) the CPI and (3) execution time, when running this code on:

a) **Single cycle CPU with clock cycle = 8ns.**

b) **Multi-cycle CPU (as covered in class - 3rd Edition Figure 5.28 page 323) with clock cycle = 2ns.**

c) **An ideal pipelined CPU with no stall cycles and clock cycle =2ns.**

d) **MIPS pipelined CPU version 1 without forwarding (4th Edition Figure 4.46 page 359 - 3rd Edition Figure 6.22 page 400) with clock cycle = 2ns.**

e) **MIPS pipelined CPU version 3 with forwarding and reduced branch delay (4th Edition Figure 4.65 page 384 - 3rd Edition Figure 6.41 page 427) and clock cycle = 2ns.**

For both non-ideal pipelined CPUs (parts d, e above) assume the branch not taken method, ignore initial pipeline fill cycles, and show resulting stall cycles.

5. **Schedule the MIPS code given in question 4 above by changing instruction order to minimize stall cycles when running on MIPS pipelined CPU version 3 with forwarding and reduced branch delay (4th Edition Figure 4.65 page 384 - 3rd Edition Figure 6.41 page 427). Assume a single branch delay slot. Show the scheduled code and provide the CPI, total number of cycles, and execution time for the scheduled code. How much faster is the scheduled code compared to the original code?**