Intel i7

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Agenda

Improvements over previous Intel Core architectures
  • Intel QuickPath Interconnect
  • Integrated Memory Controller, DMI, PCIe, Graphics
  • Turbo Boost
Second Generation i7 (Sandy Bridge)
  • Quick Sync Video
  • More Efficient Load/Store
  • Decoded Micro-op Cache
  • Improved Branch Predictor
  • Advanced Vector Extensions
Third Generation i7 (Ivy Bridge)
  • Tri-gate Transistors
Intel QuickPath Interconnect

• Point-point processor interconnect, replaces FSB
• Designed to compete with HyperTransport technology
• QPI transmits data in "flits" of 80 bits in two clock cycles
• Each "flit" has 8 bits of error detection, an 8-bit header, 64-bit data

• 5-layer architecture
  o Physical Layer: actual wiring
  o Link Layer: sends/receives control signals
  o Routing Layer: 72-bit unit: 8-bit header, 64-bit payload
  o Transport Layer: sends/receives data between QPI networks, not used in i7.
  o Protocol Layer: sends and receives packets on behalf of the device. i.e a memory cache row
DMI + PCIe and Integrated Graphics

Core 2
- FSB
- Northbridge
- DMI
- Southbridge

Core i7
- Integrated MC
- Integrated Graphics
- PCIe
- DMI
- PCH
Intel Turbo Boost Technology

Dynamically monitors processor cores to deliver optimum performance when needed.

- Commonly referred to as "Dynamic Overclocking"

Turbo Boost will only work when the processor is operating below power, current, and thermal limits.
Sandy Bridge

The Second Generation
Quick Sync Video

Hardware video encoding and decoding introduced on the Sandy Bridge platform

Quick Sync is an application-specific integrated circuit (ASIC). This allows for faster and more power efficient video processing.

Supports the H.264/MPEG-4 AVC, VC-1 and MPEG-2 video standards.
More Efficient Load/Store

Execution pipeline enhancements:

Symmetric load/store units capable of two 128-bit loads per cycle and one 128-bit store per cycle <-- a 50% increase in bandwidth compared to first generation which was limited to a single load per cycle

What does this mean?
More Efficient Load/Store continued

Serves *two* memory requests per cycle, 16 bytes load, 16 bytes store

Serves *three* memory requests per cycle, two 16 bytes loads, one 16 bytes store
Decoded Micro-op Cache

- Part of L1 cache allocated to caching decoded micro-ops

- Operation similar to regular instruction cache
  - Instruction fetched
  - Fetch hardware checks cache for decoded instruction
  - If it exists, the cache services the rest of the pipeline
  - Otherwise, instruction decoded and added to cache

- Eliminates decode step for cached instructions
  - More overall bandwidth
  - Lower latency

- Typical programs have approximately 80% hit rate
Improved Branch Predictor

• Uses a single confidence bit for multiple branches
  o Same number of bits in table for more branches
  o Leads to more accurate prediction

• More efficient branch target storage
  o Stores far away targets differently from distant targets
  o Can store more targets and increases prediction speed

• More bits for history
  o Improves prediction accuracy

• Same amount of overall storage, just more efficient
Advanced Vector Extensions

- The width of the SIMD register file doubled to 256 bits
  - Uses registers YMM0 - YMM15 (formerly XMMn)
  - Legacy SSE instructions operate on lower 128 bits of the YMM registers.

- Introduces a three-operand SIMD instruction format
  - C = A + B
  - Non-destructive
  - Reduces register load
  - Limited to YMM operands

- Increases parallelism and throughput in FP SIMD calculations.
Ivy Bridge

The Third Generation
Tri-gate Transistors

- Single 3-D gate, multiple sources/drains allow for:
  - Up to 37% higher speed
  - Up to 50% less power consumption

- Based on 22nm architecture
Miscellaneous

First generation
- On-die memory controller
- First 6 core Intel processor

Second generation (Sandy Bridge)
- AES
- Ring On-die interconnect

Third generation (Ivy Bridge)
- Random Number Generator
- The built-in GPU has up to 16 execution units (EUs)