DSP Architecture

VASU GUPTA
Overview

- Review of Digital signal Processing
- Digital Filter Example
- DSP architecture
- Speed: General processor vs DSP architecture
Digital Signal Processing

- Application of mathematical operations on digital signals
  - Algorithm must have large of mathematical operations to be performed quickly
  - And repeat on series of data samples

- Goal of DSP is measure, filter, compress signal

- Real-time Processing

- Specialized Digital Signal Processor
  - Lower-cost solution
  - Better performance
  - Lower latency
DSP Application

- Digital Audio application
- Radar
- Sonar
- Image Compression
Digital Filter Example

- Simple Filter:

\[ y[n] = \sum_{i=0}^{N-1} b_i \cdot x[n-i] \]

- Output is sum of product of coefficient and past input values.
Digital Filter (Cont.)

\[
x[n] 
\xrightarrow{Z^{-1}} x[n-1] 
\xrightarrow{Z^{-1}} x[n-2] 
\xrightarrow{Z^{-1}} x[n-3] 
\xrightarrow{+} y[n] 
\]

\[
sources: b_0 b_1 b_2 b_3 
\]
Digital Filter in DSP

- Plan of action
  - Clear Accumulator
  - Fetch coefficient and data
  - MAC
  - Repeat fetch & MAC until done
General-Purpose Processor (micro)

- Not great for DSP algorithm
  - Von Neumann architecture
    - Fetch for next instrument
    - Then another fetch data memory
    - Buses idle during instruction decode
  - 1 access/cycle
    - DSP usually have two operands for fetched
      - Coef[n]*data[n]
    - 3-7 execution cycles for Multiplying
Memory

- Von Neumann “Bottleneck”
- Most DSPs use Harvard Architecture

- Separate memories for data and program instructions, they can be fetched at same time.
DSP Architecture Feature

- ALU centered around Multiply-Accumulate (MAC)
- Large Accumulator
  - Digital Filter requires accumulated the sum of product
- Multiple address generators to handle separate memory spaces
  - Circular buffer
Accumulator

- Accumulator register holds intermediate results
- Accumulator has extra guard bits for overflow
  - Ex: 24b x 24b => 48b product, 56b Accumulator
Multiplier-Accumulator (MAC)
Circular buffer

- Circular buffer in few consecutive memory locations
- End of this linear array is connecting to its beginning
320C54x DSP
Speed: General Purpose Processor(micro) vs DSP Architecture

- ARM Cortex M3
  - 3 pipeline Stage

- ARM Cortex M4
  - M3 with DSP architecture

- Compare M3 and M4
Speed: General Purpose Processor (micro) vs DSP Architecture

- 7 band parametric EQ
- 32-bit precision
- Stereo Processing
- 48 kHz sample rate

**Performance**
- Cortex-M3 needed 1291 cycles (47.4% processor loading)
- Cortex-M4 needed only 299 cycles (11% processor loading)
Source

- http://www.dspguide.com/ch28/2.htm
- http://bwrcs.eecs.berkeley.edu/Classes/CS252/Notes/Lec09-DSP.pdf