DDR4 SDRAM

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Overview

● History
● Specifications
● Issues
● Future
● Questions
DRAM - Dynamic Random Access Memory

- Dr. Robert Dennard - IBM 1966
- Preceded by Magnetic-Core Memory Technology
- Dynamic $\rightarrow$ Volatile Memory
- 1 Transistor & 1 Capacitor per bit
  - high densities compared to SRAM
SDRAM - Synchronous Dynamic Random Access Memory

- 1970’s → popular by 2000
- Clock
- Pipeline
- Data Storage Division
- Higher Data Access Rates than DRAM
DDR1 SDRAM - Double Data Rate Synchronous Dynamic RAM

- Development in 1996, completed in 2000
- Utilizes row based structure
- Both clock edges
  - twice as fast
  - higher latency
- Reduced power consumption
DDR2

- Development completed in 2003
  - competitive in 2004
- Internal clock half speed of data bus
  - 4 data transfers per cycle
  - higher latency
- Reduced power consumption - die shrinkage
- Pin number increased
DDR3

- Specifications completed in 2007
  - A decrease in voltage from 1.8 to 1.5
  - Increased density, die shrinkage
  - Faster possible speeds (800MHz-2133MHz)
- Most common form of DRAM found today
- JEDEC Specifications have been expanded by Intel’s XMP (extreme memory profile) to enable higher speeds and performance
DDR4

- Standards published in 2012
- Only recently been made commercially available in 2014
- Standards allow for significant technological growth in the future.
- Not expected to overtake DDR3 in sales until 2016 at the earliest.
## DDR Specifications per Generation

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>1.8V to 2.5V</td>
<td>1.35V to 1.65V</td>
<td>1.2V</td>
</tr>
<tr>
<td>$V_{pp}$ Voltage</td>
<td>-</td>
<td>-</td>
<td>2.5V</td>
</tr>
<tr>
<td>Speeds</td>
<td>400, 533, 667, 800, 1066</td>
<td>800, 1066, 1333, 1600, 1866, 2133</td>
<td>2133, 2400, 2666, 2800, 3000, 3200+</td>
</tr>
<tr>
<td>IC Densities</td>
<td>512MB to 4GB</td>
<td>512MB to 8GB</td>
<td>2GB to 16GB</td>
</tr>
<tr>
<td>Internal Banks</td>
<td>8</td>
<td>8</td>
<td>16 (in banks of 4)</td>
</tr>
<tr>
<td>DIMM Densities</td>
<td>512MB to 4GB</td>
<td>512MB to 16GB</td>
<td>4GB to 32GB</td>
</tr>
<tr>
<td>Module Pins</td>
<td>240</td>
<td>240</td>
<td>288</td>
</tr>
</tbody>
</table>
Specifications

● Significant improvement in all areas when compared with DDR3.
  o Reduced voltage requirements to 1.2V, and included a secondary 2.5V supply called Vpp
  o Increased speeds (2133MHz-3200MHz and beyond)

● Low power specification still under development and is expected in 2015
Specifications Continued

- DDR4 has several protocol additions
  - Improved error correction and detection
  - The data bus has a CRC check
  - The command/address bus has a parity check
- Independent programming of DRAM’s on a DIMM for better control
- JEDEC specification includes 3D stacking for up to 8 stacked dies.
DDR Voltage per Generation

Image by Corsair
Operating Frequency per Generation

Image by Corsair
Operating Frequency over Time

Image by Corsair
Issues

• Increased latency due to larger memory sizes in DDR4
  o Offset by the significantly faster operating speeds.
Issues Continued

- Initial cost for value is worse for DDR4 when compared to DDR3 at this time
- Not backwards compatible with DDR3 DIMM slots (increase in the pin count)
- Requires significant investment in hardware upgrades
Future

● There is currently no successor to DDR4.
● Serial Memory is a strong candidate to eventually replace DDR SDRAM
  o Xilinx’s Hybrid Memory Cube (HMC)
  o MoSys’ Bandwidth Engine technology
  o Broadcom’s Ternary Content Addressable Memory
● Massively parallel Memory
  o Samsung’s High Bandwidth Memory (HBM)
Future Continued

Figure 3: Illustration of the Structure of HMC

Image by Xilinx
References


Questions