What is PCI Express?

- Peripheral Component Interconnect Express
- A high-speed serial connection
- More like a network than a bus
  - Has several point-to-point serial connections (lanes)
- Used as primary motherboard-level interconnect (host system-processor to integrated and add-on peripherals) in almost all modern PCs
- Scalable performance based on number of signal lanes implemented
History of PCI / PCI Express

• 1984-1993
  o PCs used ISA buses

• 1992
  o PCI Special Interest Group (PCI-SIG) formed

• 1993
  o PCI Introduced

• 2003
  o PCI Express 1.0a introduced
    ▪ per-lane data rate 250 MB/s

• 2007
  o PCI Express 2.0 available
PCIe vs PCI

- PCIe has a fixed width of 32 bits, can only handle 5 devices
- Every device has a dedicated connection with PCIe, don't share bandwidth like with PCI
- Connections contain fewer pins than PCI (cheaper)
- Data prioritization
- Better methods of breaking data into packets
- Flow Control
- MSI (Multiple System Interrupt) instead of the old I/O request signal
Architecture: Physical Layer

• Comes in x1, x2, x4, x8, x16, and x32 lane widths
• Bandwidth is linearly scaled by number of lanes
• Up-plugging: A PCIe device may fit in a slot its size or large (e.g. x1 device in x16 slot)
• Down-plugging: A PCIe device can fit in a smaller slot, if properly grounded (e.g. x4 device in x1 slot)
• Backwards/Forwards Compatibility:
  o PCIe 3.0 is fully compatible with previous generations.
    ▪ PCIe 1.x and 2.x cards will fit into a 3.0 slot and operate at their highest performance levels
    ▪ PCIe 3.0 cards will fit into 1.x and 2.x slots and operate at the highest performance levels
Architecture: Data Link Layer

- Primary roles:
  - Sequence the Transaction Layer Packets that are generated by the Transaction Layers
  - Ensure delivery of TLPs between endpoints (links) through acknowledgement protocol
  - Initialize/Manage flow control credits
- 12-bit sequence number and 32-bit LCRC added to TLP, and checked in this layer
  - Any errors cause TLP and possibly others to be discarded
  - LCRC protects the contents of a TLP on a link-by-link basis.
- Also generates/consumes data link layer packets
  - ACK/NAK signals, flow control credit information, and some power management messages
Architecture: Transaction Layer

• Receives read/write requests from software layer, creates request packets for transmission to link layer

• Every packet has unique identifier
  o Allows response packets to be sent to Originator

• Credit-based flow control
  o A device has a certain amount of credit for each received buffer.
  o The sending device counts the number of credits each packet would consume, and only transmits packet when it won't exceed its credit limit.
  o When the receiving device finished processing, it
Architecture: Transaction Layer

- Requests are one of four transaction types:
  - **Memory Read/Write**
    - Used to transfer data to/from a memory mapped location.
  - **I/O Read/Write**
    - Used to transfer data to/from an I/O location
  - **Configuration Read/Write**
    - Used to discover device capabilities, program features, and check status
  - **Messages**
    - Handled like posted writes. Used for event signaling and general purpose messaging.
Form Factors

Right Side:
- Pins 1-11
  (Standard PWR, SMBus and JTAG port pins)

Left Side:
- Pins 12-18 (x1)
- Pins 19-32 (x4)
- Pins 33-49 (x8)
- Pins 50-82 (x16)
[Lane 0-15 Tx/Rx Data pins]

Use same contacts
Modular body design
Use same connector manufacturing process
Form Factors (cont.)

General Applications and their Form Factors:
• x1
  o Sound Cards, Network Cards
• x4
  o Multi-Port Gigabit Cards, SATA Raid Controllers
• x8
  o Higher-end 10Gbps Gigabit Cards, SSD Raid Controllers
• x16
  o Most Graphics Cards, Co-processors (Xeon Phi)
# Performance of Earlier Buses

<table>
<thead>
<tr>
<th>Slot</th>
<th>Clock Speed</th>
<th>Number of Bits</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISA</td>
<td>4.77 MHz</td>
<td>8</td>
<td>4.77 MB/s</td>
</tr>
<tr>
<td>ISA</td>
<td>8 MHz</td>
<td>16</td>
<td>8 MB/s</td>
</tr>
<tr>
<td>MCA</td>
<td>5 MHz</td>
<td>16</td>
<td>10 MB/s</td>
</tr>
<tr>
<td>MCA</td>
<td>5 MHz</td>
<td>32</td>
<td>20 MB/s</td>
</tr>
<tr>
<td>EISA</td>
<td>8.33 MHz</td>
<td>32</td>
<td>33.3 MB/s</td>
</tr>
<tr>
<td>VLB</td>
<td>33 MHz</td>
<td>32</td>
<td>133 MB/s</td>
</tr>
<tr>
<td>AGP x1</td>
<td>66 MHz</td>
<td>32</td>
<td>266 MB/s</td>
</tr>
<tr>
<td>AGP x2</td>
<td>66 MHz</td>
<td>32</td>
<td>533 MB/s</td>
</tr>
<tr>
<td>AGP x4</td>
<td>66 MHz</td>
<td>32</td>
<td>1066 MB/s</td>
</tr>
<tr>
<td>AGP x8</td>
<td>66 MHz</td>
<td>32</td>
<td>2133 MB/s</td>
</tr>
</tbody>
</table>
## Performance of PCI / PCI-X

<table>
<thead>
<tr>
<th>Slot</th>
<th>Clock Speed</th>
<th>Number of Bits</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI</td>
<td>33 MHz</td>
<td>32</td>
<td>133 MB/s</td>
</tr>
<tr>
<td>PCI</td>
<td>33 MHz</td>
<td>64</td>
<td>266 MB/s</td>
</tr>
<tr>
<td>PCI</td>
<td>66 MHz</td>
<td>64</td>
<td>533 MB/s</td>
</tr>
<tr>
<td>PCI-X 1.0</td>
<td>66 MHz</td>
<td>64</td>
<td>533 MB/s</td>
</tr>
<tr>
<td>PCI-X 1.0</td>
<td>133 MHz</td>
<td>64</td>
<td>1066 MB/s</td>
</tr>
<tr>
<td>PCI-X 1.0</td>
<td>133 MHz</td>
<td>64</td>
<td>2132 MB/s</td>
</tr>
<tr>
<td>PCI-X 1.0</td>
<td>133 MHz</td>
<td>64</td>
<td>4266 MB/s</td>
</tr>
<tr>
<td>PCI-X 2.0*</td>
<td>266 MHz</td>
<td>64</td>
<td>2100 MB/s</td>
</tr>
<tr>
<td>PCI-X 2.0*</td>
<td>533 MHz</td>
<td>64</td>
<td>4300 MB/s</td>
</tr>
</tbody>
</table>
## Performance of PCI Express

<table>
<thead>
<tr>
<th>Slot</th>
<th>Clock Speed</th>
<th>Number of Bits</th>
<th>Bandwidth</th>
<th>Raw Bit Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe 1.x (x1)</td>
<td>2.5 GHz</td>
<td>1</td>
<td>250 MB/s</td>
<td>2.5 GT/s</td>
</tr>
<tr>
<td>PCIe 1.x (x4)</td>
<td>2.5 GHz</td>
<td>4</td>
<td>1,000 MB/s</td>
<td>2.5 GT/s</td>
</tr>
<tr>
<td>PCIe 1.x (x8)</td>
<td>2.5 GHz</td>
<td>8</td>
<td>2,000 MB/s</td>
<td>2.5 GT/s</td>
</tr>
<tr>
<td>PCIe 1.x (x16)</td>
<td>2.5 GHz</td>
<td>16</td>
<td>4,000 MB/s</td>
<td>2.5 GT/s</td>
</tr>
<tr>
<td>PCIe 2.x (x1)</td>
<td>5 GHz</td>
<td>1</td>
<td>500 MB/s</td>
<td>5.0 GT/s</td>
</tr>
<tr>
<td>PCIe 2.x (x4)</td>
<td>5 GHz</td>
<td>4</td>
<td>2,000 MB/s</td>
<td>5.0 GT/s</td>
</tr>
<tr>
<td>PCIe 2.x (x8)</td>
<td>5 GHz</td>
<td>8</td>
<td>4,000 MB/s</td>
<td>5.0 GT/s</td>
</tr>
<tr>
<td>PCIe 2.x (x16)</td>
<td>5 GHz</td>
<td>16</td>
<td>8,000 MB/s</td>
<td>5.0 GT/s</td>
</tr>
<tr>
<td>PCIe 3.0 (x1)</td>
<td>8 GHz</td>
<td>1</td>
<td>1,000 MB/s</td>
<td>8.0 GT/s</td>
</tr>
</tbody>
</table>
Encoding and Bandwidth

- Until PCIe 3.0, 8b/10b encoding was used
  - Maps each byte of data into a 10-bit symbol
  - Guarantees a deterministic DC wander and a minimum edge density over a per-bit time continuum.
  - The bit rate is specified at 5GT/s, but due to this overhead it delivers 4Gbps

- PCIe 3.0 uses a more efficient 128/130 encoding
  - Reduced overhead from the 20% loss of 8b/10b
  - Pure 128/130 encoding is about 1.5% loss
Where it Stands Today

• First v3.0 Graphics Cards released: Jan 2012

• v4.0 Final Specifications to be released in 2014/2015
  o Active and idle power optimization being investigated

• Thunderbolt: Built on 2x PCIe with DisplayPort

• CrossFire and SLI possible through high bandwidth of PCIe
Conclusion

PCI-Express is a faster, larger connection with multiple improvements over PCI, and it keeps improving. Almost all graphics cards since 2010 by ATI and NVIDIA use PCIe.
Sources

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http://www.pcisig.com/developers/main/training_materials/get_document?doc_id=db2e501c833c39720230814074816ba5b9581668
Questions?