Combinational Comparators

• Comparing two binary inputs A, B each n bits for equality (i.e. A = B) is a common operation in computers.

• A single output combinational circuit to accomplish this can be constructed using n 2-input XNOR gates for bit-wise comparison plus one n-input AND gate. The output = 1 if A = B

• This can also be done by subtraction (A - B) and checking for a zero result using a single n-input NOR gate.

• Example: 1-bit comparator: A, B 1-bit each.
  – The 1-bit comparison requires a single XNOR gate

Truth table:  Output

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>(A \oplus B)'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

1-bit comparator
Example: 4-bit Comparator

Compares \( A = A_3 A_2 A_1 A_0 \) with \( B = B_3 B_2 B_1 B_0 \)

Output = 1 if \( A = B \)
Combinational Shift Circuits

- An n-bit shift circuit (shifter) has a single n-bit data input $A$, and a single n-bit output $R$ and a number of control inputs to determine the shift amount (0 to n-1).
- Possible shift operations include:
  - Shift left or right:
    - Arithmetic right shift (the sign bit is shifted in),
    - Logic shift (0 is shifted in)
    - Rotate left or right.
- Example: Original data input $A = 11011$
  - Shift left by one: $10110$
  - Logic shift right by one: $01101$
  - Arithmetic shift right by one: $11101$
  - Rotate left by one: $10111$
- Combinational shift circuits are usually constructed using a number of levels of multiplexers.
Example: Combinational 8-Bit Right Shifter

Basic Building Block 2-to-1 Mux

A B
\[ \begin{array}{c}
1 \\
0 \\
\end{array} \]
Mux
select \( S \)

D

Three levels of Muxes used

Connect to:
- 0 for logic right shift
- or to \( A_7 \) for arithmetic right shift
- or to \( A_0 - A_6 \) for rotate right

\[ \begin{array}{cccccccc}
A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\
1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\
\end{array} \]

\[ \begin{array}{cccccccc}
R_7 & R_6 & R_5 & R_4 & R_3 & R_2 & R_1 & R_0 \\
1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\
\end{array} \]

\[ \begin{array}{cccccccc}
S_2 & S_1 & S_0 \\
1 & 0 & 1 & 0 \\
\end{array} \]
shift amount from 0 to 7

- Propagation delay: 2 gate delays per level \( \times \) 3 levels = 6 gate delays
- How many Mux levels for 32-bit shifter? Propagation delay?