Steps in Creating a Parallel Program

- 4 steps: Decomposition, Assignment, Orchestration, Mapping
- Performance Goal of the steps: Minimize resulting execution time by:
  - Balancing computations and overheads on processors (every processor does the same amount of work + overheads).
  - Minimizing communication cost and other overheads associated with each step.

(Parallel Computer Architecture, Chapter 3)
Parallel Programming for Performance

A process of Successive Refinement of the steps

• **Partitioning for Performance:**
  – Load Balancing and Synchronization Wait Time Reduction
  – Identifying & Managing Concurrency
    • Static Vs. Dynamic Assignment
    • Determining Optimal Task Granularity
    • Reducing Serialization
  – Reducing Inherent Communication
    • Minimizing $communication$ to $computation$ ratio
  – Efficient Domain Decomposition
  – Reducing Additional Overheads

• **Orchestration/Mapping for Performance:**
  – Extended Memory-Hierarchy View of Multiprocessors
    • Exploiting Spatial Locality/Reduce Artifactual Communication
    • Structuring Communication
    • Reducing Contention
    • Overlapping Communication

(Parallel Computer Architecture, Chapter 3)
Successive Refinement of Parallel Program Performance

**Partitioning** is possibly independent of architecture, and may be done first:

- View machine as a collection of communicating processors
  - Balancing the workload across processes/processors.
  - Reducing the amount of inherent communication.
  - Reducing extra work to find a good assignment.

- Above three issues are conflicting.

Then deal with interactions with architecture (Orchestration, Mapping):

- View machine as an extended memory hierarchy:
  - Extra communication due to architectural interactions.
  - Cost of communication depends on how it is structured + Hardware Architecture

- This may inspire changes in partitioning.
Partitioning for Performance

• **Balancing the workload across processes:**
  – Reducing wait time at synchronization points.

• **Reducing interprocess inherent communication.**

• **Reducing extra work needed to find a good assignment.**

These algorithmic issues have extreme trade-offs:

  – Minimize communication => run on 1 processor.
    => extreme load imbalance.

  – Maximize load balance => random assignment of tiny tasks.
    => no control over communication.

  – Good partition may imply extra work to compute or manage it

• The goal is to **compromise** between the above extremes
Load Balancing and Synch Wait Time Reduction

Limit on speedup:

\[
\text{Speedup}_{\text{problem}}(p) \leq \frac{\text{Sequential Work}}{\text{Max (Work on any Processor)}}
\]

- Work includes data access and other costs.
- Not just equal work, but must be busy at the same time to minimize synch wait time.

Four parts to load balancing and reducing synch wait time:

1. Identify enough concurrency in decomposition.
2. Decide how to manage the concurrency (statically or dynamically).
3. Determine the granularity (task grain size) at which to exploit it.
4. Reduce serialization and cost of synchronization.
Identifying Concurrency: **Decomposition**

- **Concurrency may be found by:**
  - Examining loop structure of sequential algorithm.
  - Fundamental data dependencies.
  - Exploit the understanding of the problem to devise algorithms with more concurrency (e.g. equation solver).

- **Parallelism Types:**
  - **Data Parallelism** versus **Function Parallelism**:

- **Data Parallelism:**
  - Parallel operation sequences performed on elements of large data structures
    - (e.g. equation solver, pixel-level image processing)
  - Such as resulting from parallelization of loops.
  - Usually easy to **load balance**. (e.g. equation solver)
  - Degree of concurrency usually increase with input or problem size. e.g. $O(n^2)$ in equation solver.
Identifying Concurrency (continued)

Function or Task parallelism:

- Entire large tasks (procedures) with possibly different functionality that can be done in parallel on the same or different data.
  
  e.g. different independent grid computations in Ocean.
  
  - **Software Pipelining:** Different functions or software stages of the pipeline performed on different data:
    - As in video encoding/decoding, or polygon rendering.

- **Concurrency degree usually modest** and does not grow with input size
  
  - **Difficult to load balance.**
  
  - Often used to reduce synch wait time between data parallel phases.

Most scalable parallel programs:

- (more concurrency as problem size increases) parallel programs:
  
  Data parallel (per this loose definition)
  
  - Function parallelism still exploited to reduce synchronization wait time between data parallel phases.
Levels of Parallelism in VLSI Wire-Routing Applications

Wire Parallelism

Segment Parallelism

Route Parallelism
Managing Concurrency: Assignment

Goal: Obtain an assignment with a good load balance among tasks (and processors in mapping step)

Static versus Dynamic Assignment:

Static Assignment: (e.g equation solver)
- Algorithmic assignment usually based on input data; does not change at run time.
- Low run time overhead.
- Computation must be predictable.
- Preferable when applicable (lower overheads).

Dynamic Assignment:
- Adapt partitioning at run time to balance load on processors.
- Can increase communication cost and reduce data locality.
- Can increase run time task management overheads.
Dynamic Assignment/Mapping

Profile-based (semi-static):

– Profile (algorithm) work distribution initially at runtime, and repartition dynamically.
– Applicable in many computations, e.g. Barnes-Hut, (simulating galaxy evolution) some graphics.

Dynamic Tasking:

– Deal with unpredictability in program or environment (e.g. Ray tracing)
  • Computation, communication, and memory system interactions
  • Multiprogramming and heterogeneity of processors
  • Used by runtime systems and OS too.
– Pool of tasks: take and add tasks to pool until done.
– E.g. “self-scheduling” of loop iterations (shared loop counter).
Simulating Galaxy Evolution
(Gravitational N-Body Problem)

- Simulate the interactions of many stars evolving over time
- Computing forces is expensive
  - $O(n^2)$ brute force approach
- Hierarchical Methods (e.g. Barnes-Hut) take advantage of force law: $G \left( \frac{m_1 m_2}{r^2} \right)$

- Many time-steps, plenty of concurrency across stars within one
Gravitational N-Body Problem: Barnes-Hut Algorithm

- To parallelize problem: Groups of bodies partitioned among processors. Forces communicated by messages between processors.
  - Large number of messages, $O(N^2)$ for one iteration.
- Solution: Approximate a cluster of distant bodies as one body with their total mass
- This clustering process can be applies recursively.
- Barnes_Hut: Uses divide-and-conquer clustering. For 3 dimensions:
  - Initially, one cube contains all bodies
  - Divide into 8 sub-cubes. (4 parts in two dimensional case).
  - If a sub-cube has no bodies, delete it from further consideration.
  - If a cube contains more than one body, recursively divide until each cube has one body
  - This creates an oct-tree which is very unbalanced in general.
  - After the tree has been constructed, the total mass and center of gravity is stored in each cube.
  - The force on each body is found by traversing the tree starting at the root stopping at a node when clustering can be used.
  - The criterion when to invoke clustering in a cube of size $d \times d \times d$:
    $$r \geq d/\theta$$
    $r =$ distance to the center of mass
    $\theta =$ a constant, 1.0 or less, opening angle
  - Once the new positions and velocities of all bodies is computed, the process is repeated for each time period requiring the oct-tree to be reconstructed (repartition dynamically)
Two-Dimensional Barnes-Hut

Recursive Division of Two-dimensional Space

Locality Goal:

* Bodies close together in space should be on same processor*
Barnes-Hut Algorithm

- Main data structures: array of bodies, of cells, and of pointers to them
  - Each body/cell has several fields: mass, position, pointers to others
  - Pointers are assigned to processes
Rendering Scenes by Ray Tracing

- Shoot rays into scene through pixels in image plane
- Follow their paths
  - They bounce around as they strike objects
    - They generate new rays: ray tree per input ray
- Result is color and opacity for that pixel
- Parallelism across rays.
  - Parallelism unpredictable statically.
  - Dynamic tasking needed for load balancing.
Dynamic Tasking with Task Queues

Centralized versus distributed queues.

Task stealing with distributed queues.
- Can compromise communication and data locality, and increase synchronization.
- Whom to steal from, how many tasks to steal, ...
- Termination detection (all queues empty).
- Load imbalance possible related to size of task.

(a) Centralized task queue

(b) Distributed task queues (one per process)
Performance Impact of Dynamic Assignment
On SGI Origin 2000 (cache-coherent shared distributed memory):

![Graphs showing performance impact]

- **Barnes-Hut 512k particle**
- **Ray tracing**

Legend:
- Origin, semistatic
- Challenge, semistatic
- Origin, static
- Challenge, static
- Origin, dynamic
- Challenge, dynamic

Questions:
1. What is the impact of dynamic assignment on performance?
2. How does the performance change with increasing numbers of processors for different workloads?
Assignment: Determining Task Granularity

Recall that parallel task granularity:

Amount of work or computation associated with a task.

General rule:

- **Coarse-grained** => Often less load balance
  less communication

- **Fine-grained** => more overhead; often more
  communication, contention

Communication, contention actually more affected by
mapping to processors, not just task size only.

- Overhead affected by task size too, particularly with
dynamic mapping (tasking) using task queues:
  - Small tasks -> More Tasks -> More dynamic mapping overheads.
Reducing Serialization

Careful assignment and orchestration (including scheduling)

Reducing Serialization in Event synchronization:
- Reduce use of conservative synchronization e.g.
  - point-to-point instead of barriers,
  - or reduce granularity of point-to-point synchronization (specific elements instead of entire data structure).
- But fine-grained synch more difficult to program, more synch operations.

Reducing Serialization in Mutual exclusion:
- Separate locks for separate data
  - e.g. locking records in a database instead of locking entire database: lock per process, record, or field
  - Lock per task in task queue, not per queue
  - Finer grain => less contention/serialization, more space, less reuse
- Smaller, less frequent critical sections
  - No reading/testing in critical section, only modification
  - e.g. searching for task to dequeue in task queue, building tree etc.
- Stagger critical sections in time (on different processors).
Implications of Load Balancing/Synch Time

Extends speedup limit expression to:

\[
\text{Speedup}_{\text{problem}}(p) \leq \frac{\text{Sequential Work}}{\text{Max} (\text{Work} + \text{Synch Wait Time})}
\]

Generally load balancing is the responsibility of software.

Architecture can support task stealing and synch efficiently:

- **Fine-grained** communication, *low-overhead access* to queues
  - Efficient support allows smaller tasks, better load balancing
- **Naming** logically shared data in the presence of task stealing
  - Need to access data of stolen tasks, esp. multiply-stolen tasks

=> Hardware shared address space advantageous

- Efficient support for point-to-point communication.
  - Software layers + hardware (network) support.
Partitioning for Performance:
Reducing Inherent Communication

Measure: communication to computation ratio
(c-to-c ratio)

Focus here is on interprocess communication inherent in the problem:

- Determined by assignment of tasks to processes.
- Minimize c-to-c ratio while maintaining a good load balance among processes.
- Actual communication can be greater than inherent communication.

- As much as possible, assign tasks that access same data to same process (and processor later in mapping).

- Optimal solution to reduce communication and achieve an optimal load balance is NP-hard in the general case.

- Simple heuristic partitioning solutions may work well in practice:
  - Due to specific dependency structure of applications.
  - Example: Domain decomposition
Example Assignment/Partitioning Heuristic: Domain Decomposition

- Initially used in *data parallel* scientific computations such as (Ocean) and pixel-based image processing to obtain a good load balance and c-to-c ratio.
- The task assignment is achieved by decomposing the physical domain or data set of the problem.
- Exploits the local-biased nature of physical problems
  - Information requirements often short-range
  - Or long-range but fall off with distance
- Simple example: Nearest-neighbor grid computation

\[
\text{Block Decomposition}
\]

\[
\text{Communication} = \frac{4n}{\sqrt{p}} \quad \text{Computation} = \frac{n^2}{p}
\]

\[
C_{\text{to-C}} = \frac{4\sqrt{p}}{n}
\]

\[
\text{comm-to-comp ratio} = \frac{\text{Perimeter}}{\text{Area}} \quad \text{(area to volume in 3-d)}
\]

- Depends on \(n, p\): decreases with \(n\), increases with \(p\)
Domain Decomposition (continued)

Best domain decomposition depends on information requirements

Nearest neighbor example:

- **block** versus **strip** domain decomposition:

\[
\begin{array}{cccc}
P_0 & P_1 & P_2 & P_3 \\
P_4 & P_5 & P_6 & P_7 \\
P_8 & P_9 & P_{10} & P_{11} \\
P_{12} & P_{13} & P_{14} & P_{15}
\end{array}
\]

Block Decomposition

Comm-to-comp ratio: \( \frac{4 \times \sqrt{p}}{n} \) for block, \( \frac{2 \times p}{n} \) for strip

Application dependent: strip may be better in other cases
Finding a Domain Decomposition

• **Static, by inspection:**
  – Must be predictable: grid example above, and Ocean

• **Static, but not by inspection:**
  – Input-dependent, require analyzing input structure
    • Before start of computation once input data is known.
  – E.g. sparse matrix computations, data mining

• **Semi-static (periodic repartitioning):**
  – Characteristics change but slowly; e.g. Barnes-Hut

• **Static or semi-static, with dynamic task stealing**
  – Initial decomposition based on domain, but highly unpredictable; e.g. ray tracing
Implications of Communication

- Architects must examine application latency/bandwidth needs
- If denominator in c-to-c is computation execution time, ratio gives average BW needs per task.
- If operation count, gives extremes in impact of latency and bandwidth
  - Bandwidth: assume all latency hidden.
  - Reality is somewhere in between.
- Actual impact of communication depends on structure and cost as well:
  \[
  \text{Speedup} \leq \frac{\text{Sequential Work}}{\text{Max} (\text{Work} + \text{Synch Wait Time} + \text{Comm Cost})}
  \]

→ Need to keep communication balanced across processors as well.
Partitioning for Performance: Reducing Extra Work (Overheads)

• Common sources of extra work (mainly orchestration):
  – Computing a good partition (at run time):
    e.g. partitioning in Barnes-Hut or sparse matrix
  – Using redundant computation to avoid communication.
  – Task, data distribution and process management overhead
    • Applications, languages, runtime systems, OS
  – Imposing structure on communication
    • Coalescing messages, allowing effective naming

• Architectural Implications:
  – Reduce by making communication and orchestration efficient
    (e.g. hardware support of primitives)

\[ \text{Speedup} \leq \frac{\text{Sequential Work}}{\text{Max} (\text{Work} + \text{Synch Wait Time} + \text{Comm Cost} + \text{Extra Work})} \]
Summary of Parallel Algorithms Analysis

- Requires characterization of multiprocessor system and algorithm requirements.
- Historical focus on algorithmic aspects: partitioning, mapping
- In PRAM model: data access and communication are free
  - Only load balance (including serialization) and extra work matter
  - Useful for early development, but unrealistic for real performance.
  - Ignores communication and also the imbalances it causes
  - Can lead to poor choice of partitions as well as orchestration when targeting real parallel systems.

\[
\text{Speedup} \leq \frac{\text{Sequential Instructions}}{\text{Max (Instructions + Synch Wait Time + Extra Instructions)}}
\]
Limitations of Parallel Algorithm Analysis

• **Inherent communication** in a parallel algorithm is not the only communication present:
  – **Artifactual communication** caused by program implementation and architectural interactions can even dominate.
  – Thus, actual amount of communication may not be dealt with adequately

• **Cost of communication** determined not only by amount:
  – Also how communication is structured
  – Cost of communication in system
    • Software related and hardware related (network)

• **Both architecture-dependent, and addressed in orchestration step.**
Generic Multiprocessor Architecture

Node: processor(s), memory system, plus communication assist:
  • Network interface and communication controller.
Extended Memory-Hierarchy View of Generic Multiprocessors

- **Levels in extended hierarchy:**
  - Registers, caches, local memory, remote memory (over network)
  - Glued together by communication architecture
  - Levels communicate at a certain granularity of data transfer. (e.g. Cache blocks, pages etc.)

- **Need to exploit spatial and temporal locality in hierarchy**
  - Otherwise extra communication may also be caused
  - Especially important since communication is expensive
Extended Hierarchy

- **Idealized view:** local cache hierarchy + single main memory
- But reality is more complex:
  - **Centralized Memory:** caches of other processors
  - **Distributed Memory:** some local, some remote; + network topology
  - Management of levels:
    - Caches managed by hardware
    - Main memory depends on programming model
      - SAS: data movement between local and remote transparent
      - Message passing: explicit by sending/receiving messages.
  - Improve performance through **architecture or program locality** (maximize local data access).
Artifactual Communication in Extended Hierarchy

Accesses not satisfied in local portion cause communication

- Inherent communication, implicit or explicit, causes transfers:
  - Determined by program

- Artifactual communication:
  - Determined by program implementation and architecture interactions
  - Poor allocation of data across distributed memories: data accessed heavily by one node is located in another node local memory.
  - Unnecessary data in a transfer: More data communicated in a message than needed.
  - Unnecessary transfers due to system granularities (cache block size, page size).
  - Redundant communication of data: data value may change often but only last value needed.
  - Finite replication capacity (in cache or main memory)

- Inherent communication assumes unlimited capacity, small transfers, perfect knowledge of what is needed.

- More on artifactual communication later; first consider replication-induced further
Communication and Replication

- Comm. induced by finite capacity is most fundamental artifact
  - Similar to cache size and miss rate or memory traffic in uniprocessors.
  - Extended memory hierarchy view useful for this relationship
- View as three level hierarchy for simplicity
  - Local cache, local memory, remote memory (ignore network topology).
- Classify “misses” in “cache” at any level as for uniprocessors
  - Compulsory or cold misses (no size effect)
  - Capacity misses (yes)
  - Conflict or collision misses (yes)
  - Communication or coherence misses (no)
- Each may be helped/hurt by large transfer granularity (spatial locality).
Working Set Perspective

The data traffic between a cache and the rest of the system and components data traffic as a function of cache size

- Hierarchy of working sets
- Traffic from any type of miss can be local or non-local (communication)
Orchestration for Performance

- Reducing amount of communication:
  - Inherent: change logical data sharing patterns in algorithm
    - Reduce c-to-c-ratio.
  - Artifactual: exploit spatial, temporal locality in extended hierarchy
    - Techniques often similar to those on uniprocessors

- Structuring communication to reduce cost

- We’ll examine techniques for both...
Reducing Artifactual Communication

• Message passing model
  – Communication and replication are both explicit
  – Even artifactual communication is in explicit messages
    • e.g. more data sent in a message than actually needed

• Shared address space model
  – More interesting from an architectural perspective
  – Occurs transparently due to interactions of program and system
    • Caused by sizes and granularities in extended memory hierarchy (e.g. Cache block size, page size)

• Use shared address space to illustrate issues
Exploiting Temporal Locality

- Structure algorithm so working sets map well to hierarchy
  - Often techniques to reduce inherent communication do well here
  - Schedule tasks for data reuse once assigned
- Multiple data structures in same phase
  - e.g. database records: local versus remote
- Solver example: blocking

- More useful when \( O(n^{k+1}) \) computation on \( O(n^k) \) data
  - Many linear algebra computations (factorization, matrix multiply)
Exploiting Spatial Locality

• Besides capacity, granularities are important:
  – Granularity of allocation
  – Granularity of communication or data transfer
  – Granularity of coherence

• Major spatial-related causes of artifactual communication:
  – Conflict misses
  – Data distribution/layout (allocation granularity)
  – Fragmentation (communication granularity)
  – False sharing of data (coherence granularity)

• All depend on how spatial access patterns interact with data structures
  – Fix problems by modifying data structures, or layout/alignment

• Examine later in context of architectures
  – One simple example here: data distribution in SAS solver

Larger when farther from processor
Spatial Locality Example

- Repeated sweeps over elements of 2-d grid, block assignment, Shared address space;
- Distributed memory. A memory page is allocated in one node's memory;
- Natural 2-d versus higher-dimensional array representation

**Ex: (1024, 1024)**

(a) Two-dimensional array

Page straddles partition boundaries: difficult to distribute memory well

Cache block straddles partition boundary

**Ex: (4, 4, 256, 256)**

(b) Four-dimensional array

Page does not straddle partition boundary

Cache block is within a partition

(generates more artifactual communication)
Execution Time Breakdown for Ocean on a 32-processor Origin2000

1026 x 1026 grids with block partitioning on 32-processor Origin2000

4-d grids much better than 2-d, despite very large caches on machine (4MB L2 cache)
- data distribution is much more crucial on machines with smaller caches

Major bottleneck in this configuration is time waiting at barriers
- imbalance in memory stall times as well

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<th>Time (s)</th>
<th>Data</th>
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<th>Busy</th>
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<td>4</td>
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</tbody>
</table>

Speedup = 6/3.5 = 1.7

Four-dimensional arrays
- Two-dimensional arrays
Tradeoffs with Inherent Communication

Partitioning grid solver: blocks versus rows
- Blocks still have a spatial locality problem on remote data
- Row-wise (strip) can perform better despite worse inherent c-to-c ratio

• Result depends on $n$ and $p$

Results to show this next
Example Performance Impact

Equation solver on SGI Origin2000 (distributed shared memory)

**rr** = Round Robin Page Distribution

**Rows** = Strip Assignment

---

**Graphs:**

1. **Speedup vs. Number of Processors**
   - **Rows**
   - **4D**
   - **2D**

   **514 x 514 grids**

2. **Speedup vs. Number of Processors**
   - **4D**
   - **4D-rr**
   - **Rows**
   - **Rows-rr**
   - **2D**
   - **2D-rr**

   **12k x 12k grids**

---

**Ideal Speedup**

**Super-linear Speedup**
Structuring Communication

Given amount of comm (inherent or artifactual), goal is to reduce cost

- Cost of communication as seen by process:

\[ C = f \times ( o + l + \frac{n_c}{m} + t_c - \text{overlap}) \]

- \( f \) = frequency of messages
- \( o \) = overhead per message (at both ends)
- \( l \) = network delay per message
- \( n_c \) = total data sent
- \( m \) = number of messages
- \( B \) = bandwidth along path (determined by network, NI, assist)
- \( t_c \) = cost induced by contention per message
- \( \text{overlap} \) = amount of latency hidden by overlap with comp. or comm.

- Portion in parentheses is cost of a message (as seen by processor)
- That portion, ignoring overlap, is latency of a message
- Goal: reduce terms in communication latency and increase overlap
Reducing Overhead

- Can reduce number of messages $m$ or overhead per message $o$

- Message overhead, $o$ is usually determined by hardware and system software
  - Program should try to reduce number of messages $m$ by **combining messages**.
  - More control when communication is explicit (message-passing).

- **Combining data into larger messages:**
  - Easy for regular, coarse-grained communication
  - Can be difficult for irregular, naturally fine-grained communication.
    - May require changes to algorithm and extra work
      - Combining data and determining what and to whom to send.
Reducing Network Delay

- Total network delay component = \( f^* l = f^* h^* t_h \)
  - \( h = \) number of hops traversed in network
  - \( t_h = \) link+switch latency per hop
- Reducing \( f \): Communicate less, or make messages larger
- Reducing \( h \):
  - Map communication patterns to network topology
    e.g. nearest-neighbor on mesh and ring etc.
  - How important is this?
    - Used to be a major focus of parallel algorithm design
    - Depends on number of processors, how \( t_h \), compares with other components, network topology and properties
    - Less important on modern machines
      - (Generic Parallel Machine)
Reducing Contention

- All resources have nonzero occupancy (busy time):
  - Memory, communication controller, network link, etc.
    - Can only handle so many transactions per unit time.
    - Results in queuing delays at the busy resource.

- Effects of contention:
  - Increased end-to-end cost for messages.
  - Reduced available bandwidth for individual messages.
  - Causes imbalances across processors.

- Particularly insidious performance problem:
  - Easy to ignore when programming
  - Slows down messages that don’t even need that resource
    - By causing other dependent resources to also congest
  - Effect can be devastating: Don’t flood a resource!
Types of Contention

- Network contention and end-point contention (*hot-spots*)
- *Location* and *Module* Hot-spots
  - Location: e.g. accumulating into global variable, barrier
    - solution: tree-structured communication
  - Module: all-to-all personalized comm. in matrix transpose
    - Solution: stagger access by different processors to same node temporally
  - In general, reduce burstiness; may conflict with making messages larger
Overlapping Communication

• Cannot afford to stall for high latencies
• Overlap with computation or communication to hide latency
• Techniques:
  – Prefetching (start access or communication before needed)
  – Block data transfer
  – Proceeding past communication (e.g. non-blocking receive)
  – Multithreading (switch to another ready thread or task)

• In general these techniques require:
  – Extra concurrency per node (slackness) to find some other computation.
  – Higher available bandwidth (for prefetching).

More on these techniques in PCA Chapter 11
Summary of Tradeoffs

• Different goals often have conflicting demands
  – Load Balance
    • Fine-grain tasks
    • Random or dynamic assignment
  – Communication
    • Usually coarse grain tasks
    • Decompose to obtain locality: not random/dynamic
  – Extra Work
    • Coarse grain tasks
    • Simple assignment
  – Communication Cost:
    • Big transfers: amortize overhead and latency
    • Small transfers: reduce contention
# Relationship Between Perspectives

<table>
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<th>Parallelization step(s)</th>
<th>Performance issue</th>
<th>Processor time component</th>
</tr>
</thead>
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<td>Decomposition/assignment/orchestration</td>
<td>Load imbalance and synchronization</td>
<td>Synch wait</td>
</tr>
<tr>
<td>Decomposition/assignment</td>
<td>Extra work</td>
<td>Busy-overhead</td>
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<td>Decomposition/assignment</td>
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<td>Orchestration</td>
<td>Artifactual communication and data locality</td>
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<tr>
<td>Orchestration/mapping</td>
<td>Communication structure</td>
<td></td>
</tr>
</tbody>
</table>
Components of Execution Time From Processor Perspective

(a) Sequential
(b) Parallel with four proc
Summary

\[ \text{Speedup}_{\text{prob}}(p) = \frac{\text{Busy}(1) + \text{Data}(1)}{\text{Busy}_{\text{useful}}(p) + \text{Data}_{\text{local}}(p) + \text{Synch}(p) + \text{Data}_{\text{remote}}(p) + \text{Busy}_{\text{overhead}}(p)} \]

- Goal is to reduce denominator components
- Both programmer and system have role to play
- Architecture cannot do much about load imbalance or too much communication
- But it can:
  - reduce incentive for creating ill-behaved programs (efficient naming, communication and synchronization)
  - reduce artifactual communication
  - provide efficient naming for flexible assignment
  - allow effective overlapping of communication